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" Implimentation of SD Processor Based On CRDC Algorithm "

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Abstract: *In Digital Signal Processing (DSP) there are many complex algorithms for which an efficient hardware implementation is required in real time applications. One such complex algorithm is Singular-value Decomposition (SD) which is an important algorithm with applications in varied domains of signal processing such as direction estimation, spectrum analysis and systems identification. It is a generalized extension to the eigen-decomposition for non-square matrices and is hence of great importance, particularly for subspace based algorithms in signal processing. But SD is known to be a very complicated algorithm with computational complexity ~O(N^3) (for a NxN square matrix). For real-time computation of such a complex algorithm the use of a parallel and direct mapped hardware solution is indeed desired.*
Hardware and software resources:
1. *OS: Windows 9x or upper*
2. *RAM : Minimum 512 MB*
3. *Programming Language: XILINX 8.6 or upper (VERILOG)*

I. Introduction

In this chapter basic idea of the project undertaken is explained. Starting from the aim of the project, Importance and the problem associated with the design is also discussed. Finally line of approach to solve the problem is presented and organization of rest of the report is briefly shown.

Importance

The Singular Value Decomposition (SD) is an important matrix factorization with applications in signal processing, image processing and robotics. It is generally acknowledged that the SD is the only generally reliable method for determining the rank of a matrix numerically. The SD is a very useful tool, for example, in analyzing data matrices from sensor arrays for adaptive beam forming , and low rank approximations to matrices in image enhancement . The wide variety of applications for the SD coupled with its computational complexity justifies dedicating hardware to this computation. Designed 2X2 CRDC based SD processor can be used as basic building block for an array of processors of N X N matrix.

Problem statement

The importance of hardware implementation is now known but there are certain complexities that come on the way of implementation. In a typical computer algorithm for the SD, the sines and cosines of the rotation angles are computed through formulas that require division and square root operations. Also the explicit angles are not required and only thesines and cosines are computed. The rotations are then applied to the 2x 2 sub-matrix using standard matrix multiplication techniques. But in this method many time-consuming operations such as multiplication, division, and square rootare needed.
The SD is more closely mapped ontohardware through the useof the CRDC algorithms. CRDC algorithm provides an iterative scheme, consisting of simple addition and binary shift operations, to compute trigonometric values to any desired precision. The CRDC algorithms can provide the calculation of vector rotation and inverse tangent without costly hardware that proves very beneficial for implementation of SD processor.

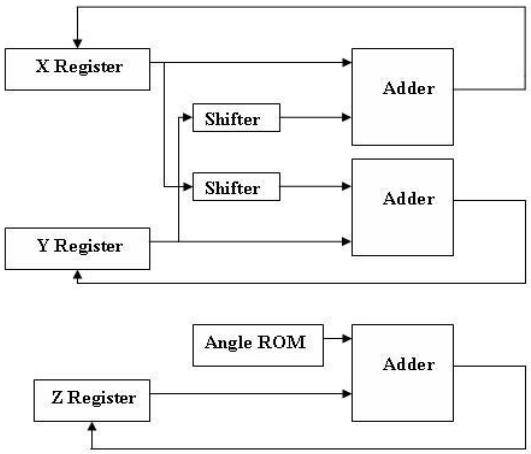
Line of approach

The complexity of SD computation and its real-time applications were the inspiration behind efficient hardware implementation. In SD processor time consuming operations like multiplication, square root and division are eliminated by the use of CRDC algorithm. CRDC algorithm only requires simple shift and additions which efficiently maps SD processor.

Basic CRDC architecture

An iterative CRDC architecture can be obtained simply by duplicating each of the three difference equations in hardware as shown in Figure.

Figure: Basic CRDC hardware



The decision function, d_i is driven by the sign of the y or z register depending on whether it is operated in rotation ($\mathbf{z}_i$) or vectoring mode (y_i). In operation, the initial values are loaded via multiplexers into the x, y and z registers. Then on each of the next n clock cycles, the values from the registers are passed through the shifters and adders-subtractors and the results placed back in the registers. The shifters are modified on each iteration to cause the desired shift for the iteration. Likewise, the ROM (Look-up table) address is incremented on each iteration so that the appropriate elementary angle value is presented to the z adder-subtractor.

On the last iteration, the results are read directly from the adder-subtractors. A simple state machine is required to keep track of the current iteration, and to select the degree of shift and ROM address for each iteration.As shown above, CRDC iteration requires 2 shifters, 1 table lookup and 3 adders. For n bits of precision, n iterations are needed.

II. Conclusion

In linear algebra, the singular value decomposition (SD) is an important factorization of a rectangular real or complex matrix, with several applications in signal processing and statistics.

A 2X2 CRDC based SD processor was designed and successfully simulated. CRDC algorithm was used to simplify the computational complexities of SD calculation. Apart from calculating the SD of a 2x2 matrix the processor is able to calculate basic CRDC functions also that are sine/cosine, inverse Tan.

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