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# Asynchronous Viterbi Decoder Using Four Phase Handshake Protocol

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***Abstract:*** *In this paper design of asynchronous Viterbi decoder is shown. Various protocols can be use to design asynchronous digital system. Bundle data protocol is one of them which are being used here to design decoder. Asynchronous Viterbi decoder for code rate ½ and constraint length 3 is designed using Xilinx 13.1. Four phase bundled data protocol is used because of its simplicity of designing to reduce the dynamic power of decoder. Register exchange method is well known method used for the design of Viterbi decoder. Here results are compared with the two different methods of decoder design. Hybrid register exchange method is being outperforms than register exchange method as this helps in reducing switching activity and hence the dynamic power. Proposed HRE method helps to reduce average dynamic power by 16.95% than proposed RE method designed using four phase handshaking protocol. XPower analyzer tool of Xilinx13.1 is used to calculate the dynamic power.*

***Keywords:*** *Viterbi Decoder, Viterbi Algorithm, REM, HREM, ACS, Handshaking*

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## I. Introduction

From many years researchers are doing research on asynchronous logic and its design implementation. Some of the advantages of asynchronous design over synchronous are low power, high speed, low electromagnetic interference and no clock skew problem. Speed have been always inspiring parameter for today's high speed applications. Here we are discussing on low power applications design. In this paper low power asynchronous Viterbi decoder is being discussed. Viterbi decoder can be designed by different design methods. Register exchange and trace back method are the two well known methods for decoding data. But in RE continuous switching have to perform by decoder which results in increased switching activity and hence the dynamic power. TB method requires last in first out register in backward tracing due to addition in LIFO; TB method also consumes more dynamic power. By adding both RE and TB methods new designed method is known as hybrid register exchange method. In HRE switching activity is reduced which helps in reducing the dynamic power.

Asynchronous circuits are being attractive for battery operated devices because of the elimination of global clock signal. Asynchronous system uses two additional wires for synchronizing different blocks in the circuit. This is called as handshake protocol. Bundled data asynchronous circuits are similar to synchronous circuits. It replaces the global clock by local handshake protocol. Handshake protocol consists of two phase and four phase protocols. This paper is divided into several sections as; Section 2 gives a brief description about signaling protocol used in bundle data handshaking. Section 3 details the proposed Asynchronous Viterbi decoder followed by Results & discussion in section 4. A conclusion will found in section 5.

## II. Signaling Protocol

For designing asynchronous circuits there are many models and methodologies are in existents. These can be categories as signaling protocol, data encoding protocol and delay insensitive protocol. First asynchronous design style is called quasi delay insensitive (QDI) [1] design. QDI design relies on dual rail scheme. These designs require large area and have high switching activity when compared with its synchronous counterpart. Another style is bundle data which relies on delay lines. This design has advantages as reduced in switching activity along with area. This style relies on complex set of timing assumptions it faces technology related problems [2].

To synchronies the different blocks of asynchronous design need local clock. This local clock use in signaling protocol as handshake signal. Signaling protocol consists of two phase and four phase handshaking. Handshaking is well known protocol for designing asynchronous system.

- **Two Phase Handshake**

An asynchronous design supports the handshaking protocol. Two phase handshaking acts on rising or falling edge of local request signal. . In this signaling scheme, the operation occurs is (1) data available (2) change request to high (active) state (3) Change acknowledge to high (active) state. As shown in figure 1; when valid data is available request become 1, after delay acknowledgement become 1 and data can be transmitted. Two phase protocol is also called as non return to zero protocol as it is edge triggered. Therefore both the rising and falling edges of handshake signals show a new activity on the related signal. Two phase style can only be used in bundled data communication. Two phase systems can be faster than four phase as they uses non return to zero phases. But circuit require to implement this protocol is more complicated.

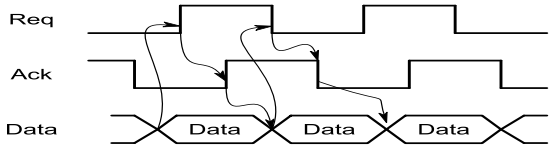


**Figure 1:** Two Phase Handshake Protocol

- **Four Phase Handshake**

Four phase protocol [1] is one of the methods of communicating between computing units in asynchronous system. Four phase bundled data protocol is most commonly used handshaking protocol. Activity while transmission of data using four phase handshake protocol is shown in figure 2. In this signaling scheme, the operation occur is (1) data available (2) change request to high (active) state (3) Change acknowledge to high (active) state (4) return request to low (inactive) state (5) return acknowledge to low (inactive) state [3].

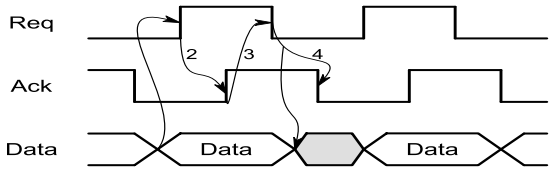


**Figure 2:** Four-Phase Handshake Protocol

When four-phase signaling is used there is a choice to be made as to which edge (rising or falling) of each handshake signal is active and takes the place of the event described above; the other edge is inactive and is part of the recovery phase during which the circuit prepares for the next cycle.

## III. Proposed Asynchronous Viterbi Decoder Design

Viterbi decoder is assumed to be best decoding algorithm for convolutional encoded data. It comprises of three basic units as BMU, ACS and SMU as shown in figure 3. The BMU computes the branch metric of each branch of the trellis. Each branch metric is recursively added to the corresponding state metric, in the State Metric Unit (SMU), to generate the new state metric. The Add-Compare-Select unit receives two branch metrics and the state metrics. An ACS module adds each incoming branch metric of the state to the corresponding state metric and compares the two results to select a smaller one. The survivor path unit records the survivor path of each state selected by the ACS module. Once the trellis diagram is reconstructed, tracing back through the trellis is performed.

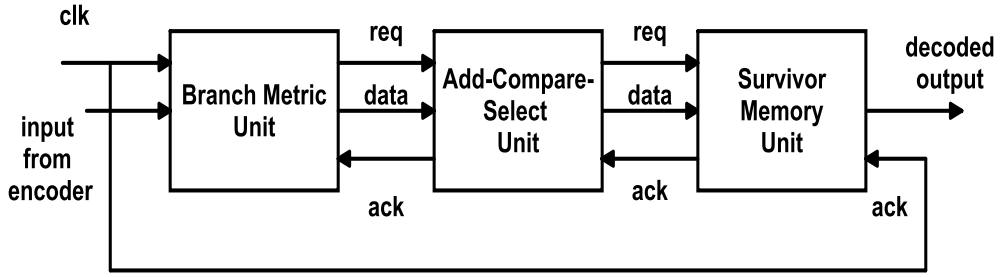


**Figure 3**: Proposed Asynchronous Viterbi Decoder.

In the Viterbi decoder; register-exchange method is used to decode the encoded data in survivor path unit. Register exchange method perform continuous switching and hence for long constraint length it is not used. Proposed method designed for decoding data bits is known as hybrid register exchange method (HREM) [4]. Switching activity can be reduced using this method. The initial state can be first traced through an m cycle, and then transfer the content of initial state to the current state and the next m bits of the register is the m bits of current state itself.

RTL View of proposed self timed asynchronous Viterbi decoder using four phase handshake protocol is depicted in figure 5. Output of the encoder is given to noise to generate noisy signal. These noisy signals are given as input to BMU where branch metrics are calculated using hamming distance property. ACSU unit plays vital role in Viterbi decoder. Here BM adds to the corresponding PM & generates new PM. New PM is compared with old PM & then store in PMM. ACSU store associated survivor path decision in the SMU. Two separate request and acknowledgement signal are used to synchronize all different blocks of decoder. SMU keep the track of data exchange.

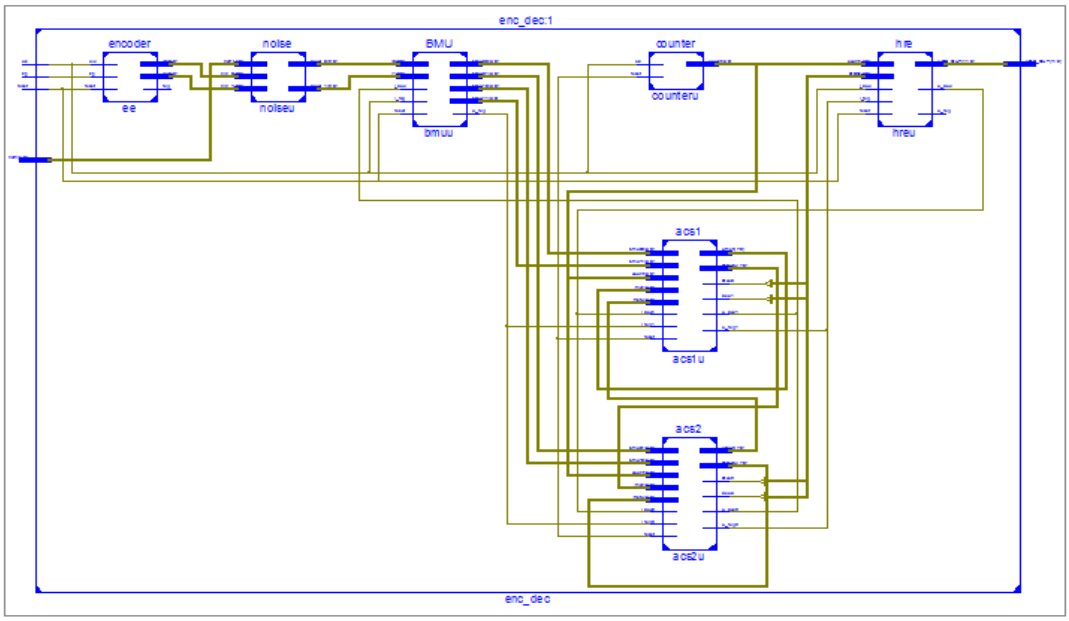


**Figure 4**: RTL View of Asynchronous Viterbi Decoder Using HRE Method

From the Figure 5, associated with each trellis state S at time t is a path metric $PM_t(p)$ and $PM_t(q)$ which is the accumulated metric along the shortest path leading to that state. The path metrics at time t can be recursively calculated in terms of path metrics of the previous iteration using equation 1 & equation 2.

$$PM_t(p) = \min\left(PM_{t-1}(i) + BM_t(i,p), PM_{t-1}(j) + BM_t(j,p)\right) \quad ---\ equation\ (1)$$

$$PM_t(q) = \min\left(PM_{t-1}(j) + BM_t(j,q), PM_{t-1}(i) + BM_t(i,q)\right) \quad ---\ equation\ (2)$$

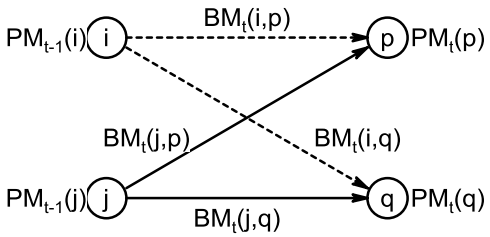


**Figure 5:** Butterfly structure

## IV. Results & Discussion

Four phase handshaking protocol is used to design the Viterbi decoder. Control signals are generated from the counter to synchronize each blocks of VD asynchronously. Asynchronous Viterbi decoder is designed using register exchange and hybrid register exchange method. Figure 6 and 7 shown are output waveform of asynchronous VD using REM and HREM respectively. VD is designed in VHDL using Xilinx ISE design Suite 13.1.

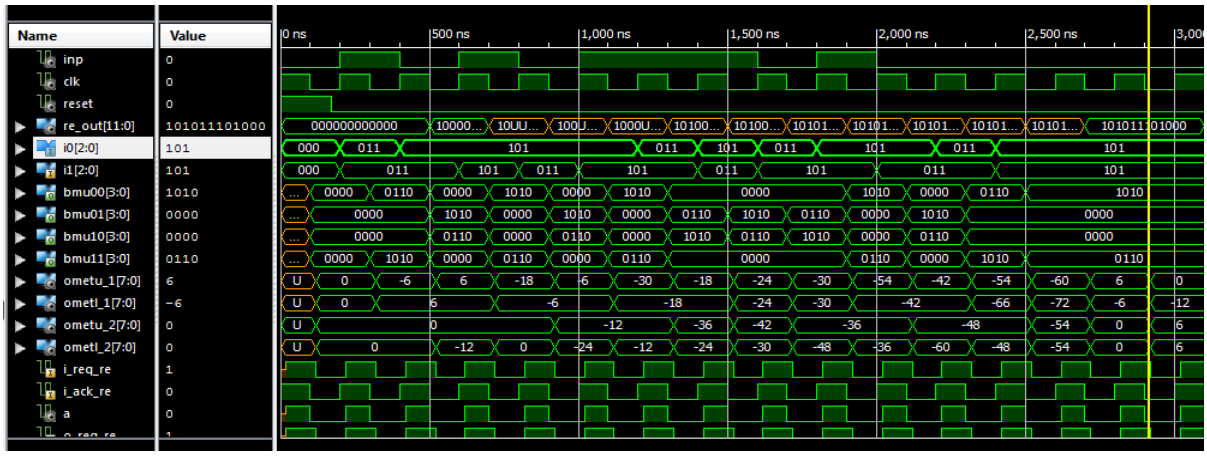


**Figure 6:** Simulation Results of Asynchronous Viterbi Decoder Using REM

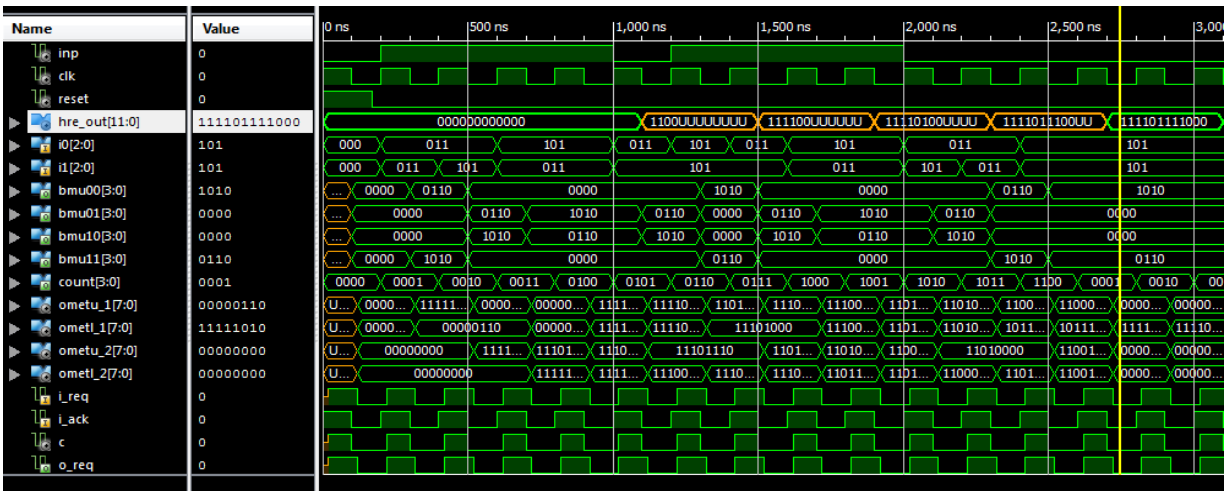


**Figure 7:** Simulation Results of Asynchronous Viterbi Decoder Using HREM

Dynamic power calculation of Viterbi decoder is done for fifteen different inputs sequences. Average dynamic power is calculated using the obtained results. Figure 8 shows the comparative analysis of average dynamic (signal and logic) power for synchronous and proposed asynchronous designs using register exchange and hybrid register exchange method. From the graph shown in figure 8 it is clear that dynamic power dissipation of asynchronous VD using HRE method is very low as compared to other all methods.

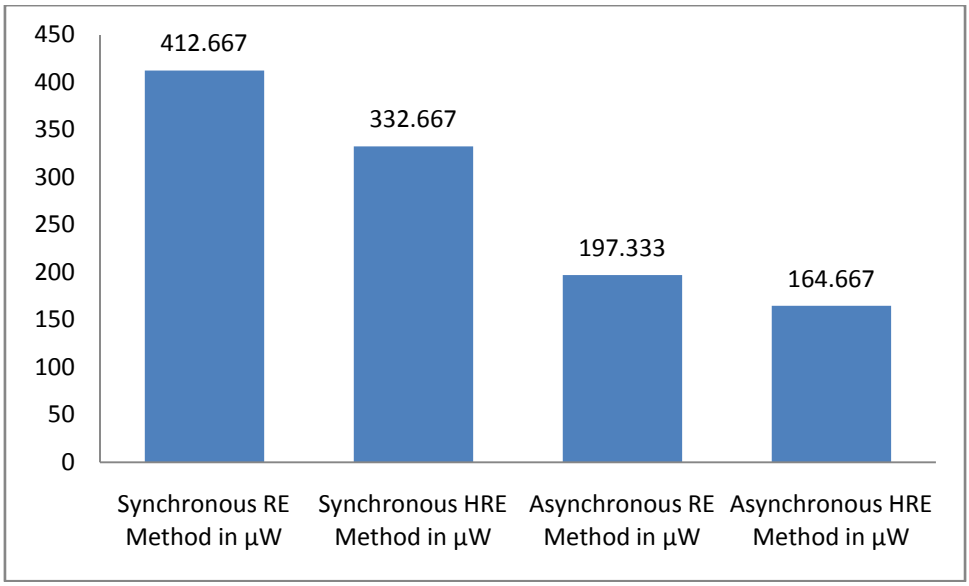


**Figure 7:** Comparative Analysis of Average Dynamic Power for Synchronous and Proposed Asynchronous Method

## V. Conclusion

In this paper asynchronous Viterbi decoder designed using four phase single rail handshake protocol is presented. Two different decoding methods are considered for design of Viterbi decoder viz. Register exchange and Hybrid register exchange. A four state, 1/2- code rate with constraint length of 3 Viterbi decoder is designed. Average dynamic power is reduced by 52.18% in proposed asynchronous RE method when compared with its synchronous counterpart. Whereas in proposed HREM average dynamic power is reduced by 50.50% when compared with synchronous HRE method. In proposed HRE method average dynamic power is reduced by 16.55% with improvement in system performance when compared with proposed RE method. The complete design is carried out using VHDL and power is calculated using XPower analyzer in Xilinx ISE design Suite 13.1.

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