International Journal of Engineering Science Invention (IJESI)
ISSN (Online): 2319 – 6734, ISSN (Print): 2319 – 6726
www.ijesi.org ||Volume 7 Issue 2Ver III || February 2018 || PP. 10-38

Power Minimisation in Scan Sequential Circuits Based On Best Primary Input Change Time

Prof.Dr.G.Manoj Someswar[1], B.Babu Rajesh[2]
1. Research Supervisor, Dr.APJ Abdul Kalam Technical University, Lucknow, U.P., India
2. Research Scholar, Dr.APJ Abdul Kalam Technical University, Lucknow, U.P., India
Corresponding Author: Prof.Dr.G.Manoj Someswar

Abstract: Testing low power very large scale integrated (VLSI) circuits in the recent times has become a critical problem area due to yield and reliability problems. This research work lays emphasis on reducing power dissipation during test application at logic level and register-transfer level (RTL) of abstraction of the VLSI design flow. In the initial stage, this research work addresses power reduction techniques in scan sequential circuits at the logic level of abstraction.

Implementation of a new best primary input change (BPIC) technique based on a novel test application strategy has been proposed. The technique increases the correlation between successive states during shifting in test vectors and shifting out test responses by changing the primary inputs such that the smallest number of transitions is achieved. The new technique is test set dependent and it is applicable to small to medium sized full and partial scan sequential circuits. Since the proposed test application strategy depends only on controlling primary input change time, power is reduced with no penalty in test area, performance, test efficiency, test application time or volume of test data. Furthermore, it is indicated that partial scan does not provide only the commonly known benefits such as less test area overhead and test application time, but also less power dissipation during test application when compared to full scan. With a view to promote for power savings in large scan sequential circuits, a new test set independent multiple scan chain-based technique which employs a new design for test (DFT) architecture and a novel test application strategy has been indicated in this research work. The technique has been validated using benchmark examples and it has been shown that power is reduced with low computational time, low overhead in test area and volume of test data and with no penalty in test application time, test efficiency, or performance. The second part of this dissertation addresses power reduction techniques for testing low power VLSI circuits using built-in self-test (BIST) at RTL. First, it is important to overcome the shortcomings associated with traditional BIST methodologies. It is shown how a new BIST methodology for RTL data paths using a novel concept called test compatibility classes (TCC) overcomes high test application time, BIST area overhead, performance degradation and volume of test data, fault-escape probability, and complexity of the testable design space exploration. Secondly, power reduction in BIST RTL data paths is achieved by analyzing the effect of test synthesis and test scheduling on power dissipation during test application and by employing new power conscious test synthesis and test scheduling algorithms. Thirdly, the innovative BIST methodology has been validated using benchmark examples. Also, the research work states that when the power conscious test synthesis along with the test scheduling is combined with novel test compatibility classes and in this proposed research work, simultaneous reduction in test application time and power dissipation is achieved with low overhead in computational time.

Keywords: *Best primary input change (BPIC), Design for testability (DFT), Scan chain, Register-transfer level (RTL), Power Dissipation Model*

Date of Submission: 09-02-2018 Date of acceptance: 24-02-2018

I. Introduction

The most important design for testability (DFT) method, at the logic level of abstraction, employed for increasing the testability of VLSI circuits is the scan-based DFT method. The scan-based DFT method makes sequential elements (latches or flip flops) controllable and observable by chaining them into a shift register (scan chain). Early test automation approaches have inserted scan is after the preliminary stages of gate placement and routing were completed. However, due to the increasing complexity of very deep sub-micron VLSI circuits scan chains need to be inserted in a structural network of logic gates at the logic level of abstraction of the VLSI design flow. Therefore, the best exploration of alternative solutions for power minimisation in scan sequential circuits is most effectively done at the logic level of abstraction. This is illustrated in Figure 1 where scan cells can be inserted either prior to or after the logic optimisation phase. The design is specified in a hardware description language (HDL) (either VHDL or Verilog) at the register-transfer

level (RTL) of abstraction of the VLSI design flow and RTL synthesis translates the initial design into a network of logic gates before logic optimisation satisfies the area and delay constraints, and prepares the design for the physical design automation tools.

This chapter addresses power minimisation during test application in small to medium sized scan sequential circuits by analysing and exploiting the influence of primary input change time on the minimisation of power dissipation during test application. A new test application strategy based on best primary input change (BPIC) time in scan sequential circuits is introduced. Furthermore, the effect of combining the primary input change time with test vector and scan cell ordering on power dissipation is investigated. The proposed test application strategy depends only on controlling the primary input change time, and hence minimises power dissipation during test application with no penalty in test area, performance, test efficiency, test application time or volume of test data. The rest of the chapter is organised as follows. It gives the motivation and objectives of the proposed research. The power dissipation model and the parameters which are accountable for power dissipation in scan circuits during test application are described. It explains why the primary input change time has strong impact on reducing spurious transitions during test application. New algorithms for exploiting all the parameters which lead to considerable savings in power dissipation are introduced in research paper. Experimental results and a comparative study of full scan and partial scan from the power dissipation standpoint are presented.

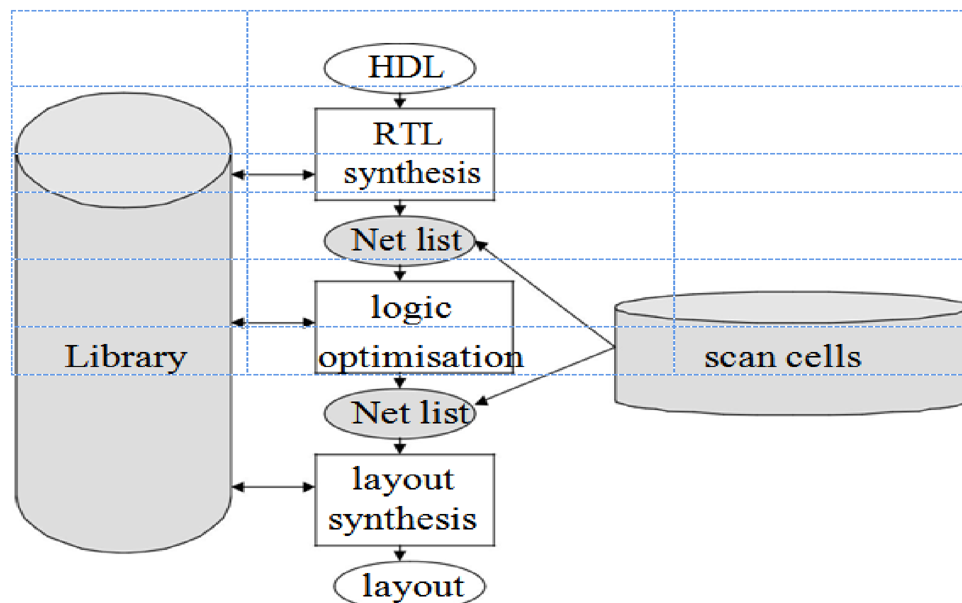


Figure 1: Logic level scan insertion

II. Motivation And Objectives

To reduce the complexity of ATPG for sequential circuits structured DFT is required. When all the sequential elements are chained into a shift register, the full scan DFT method is employed. Design teams use an existing family of scan cells from a standard cell library developed by a semiconductor manufacturer or third-party library vendor. Although full scan reduces the complexity of ATPG for sequential circuits to ATPG for combinational circuits, which is more tractable, there are three main shortcomings associated with full scan design: increase in critical path delays which leads to performance degradation; increase in test area due to extra hardware; long test application due to serial shifting of test patterns and responses. To reduce performance degradation, test area over-head and test application time associated with full scan, partial scan was proposed. The main attribute of partial scan DFT method is to select a small number of scan cells which allows ATPG to achieve a high fault coverage in a low computational time. Most of the previous approaches proposed to reduce power dissipation in scan sequential circuits introduce further over-head in performance, area or test application time. The only technique for power minimisation in full scan sequential circuits with no penalty in test area, performance, test efficiency, test application time or volume of test data was proposed in. This technique is based on test vector ordering and scan cell ordering. On the one hand, test vector ordering proposed in is efficient for full scan, but it is prohibited for partial scan. This is due to the fact that testing partial scan sequential circuits is a combination of testing full scan and non-scan sequential circuits where fixed test vector order fault activation and fault-effect propagation sequences through non-scan cells are required. On the other

hand, scan cell ordering was previously used to improve coverage of delay faults in skew-load delay fault testing, to reduce test application time, and to minimise routing area overhead. However, scan cell ordering proposed in is test set dependent and targets minimisation of power dissipation during test application. A test set dependent approach for power minimisation depends on the size and the value of the test vectors in the test set. This is unlike the test set independent approaches, where power minimisation depends only on the circuit structure and savings are guaranteed regardless of the size and the value of the test vectors in the test set. Finally, the technique proposed in is applicable only to full scan sequential circuits, due to test vectoring and did not consider the effect of the timing of the primary input part of the test vector on the power dissipation during test application.

This research work proposes a new test set dependent test application strategy which is applicable to both full scan and partial scan sequential circuits with no penalty in test area, performance, test efficiency, test application time or volume of test data. It is also shown that the smaller number of scan cells in partial scan sequential circuits leads not only to commonly known less test area overhead and test application time, but also to less power dissipation during test application and computational time required for design space exploration when compared to full scan sequential circuits.[1]

Power Dissipation During Test Application

It introduces the power dissipation model used by the techniques and algorithms presented in reviews scan cell and test vector ordering proposed by previous research for full scan sequential circuits, and investigates the applicability of scan cell and test vector ordering for partial scan sequential circuits.

Power Dissipation Model

Total power dissipation in CMOS circuits can be divided into static, short circuit, leakage and dynamic power dissipation. The static power dissipation is negligible for correctly designed circuits. Short circuit power dissipation caused by short circuit current during switching and power dissipated by leakage currents contribute up to 20% of the total power dissipation. The remaining 80% is attributed to dynamic power dissipation caused by switching of the gate outputs. If the gate is part of a synchronous digital circuit controlled by a global clock, it follows that the dynamic power P_d required to charge and discharge the output capacitance load of every gate is:

$$P_d = 0{:}5 \quad C_{load} \quad (V_{DD}^2 = T_{cyc}) \; N_G \qquad (1)$$

Where C_{load} is the load capacitance, V_{DD} is the supply voltage, T_{cyc} is the global clock period, and N_G is the total number of gate output transitions (0 ! 1 and 1 ! 0). The vast majority of power reduction techniques concentrate on minimising the dynamic power

Scan In

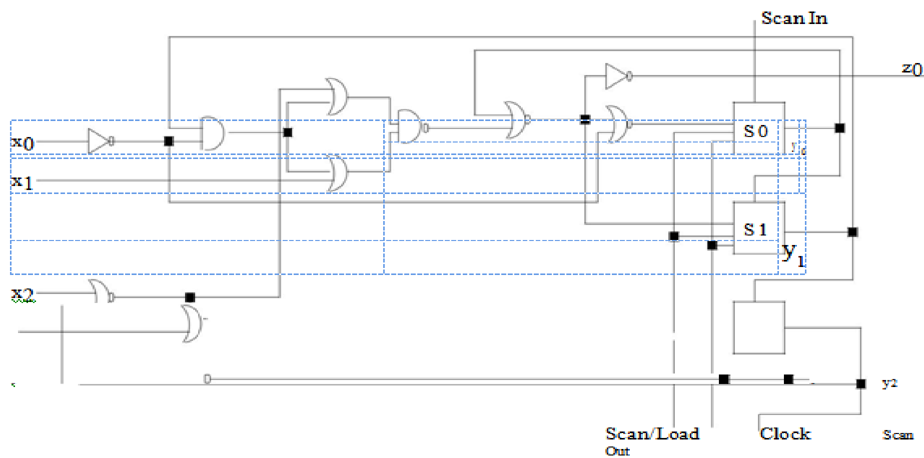


Figure 2: Example 1 circuit

dissipation P_d by minimising switching activity. Thus, node transition count

$$NT\,C = \quad å \quad {}^{N}G^{C}load \qquad (3.2)$$

□ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □

is used as quantitative measure for power dissipation throughout this chapter. It is assumed that the load capacitance for each gate is equal to the number of fan outs. The node transition count in scan cells, N_{SC} , is considered as in, where it was shown that for input changes 0 ! 0 and 1 ! 1, N_{SCmin} = 2, whilst for input changes 0 ! 1 and 1 ! 0, N_{SCmax} = 6. Similarly, the node transition count in non-scan cells, N_{NSC} , is considered N_{NSCmin} = 1 and N_{NSCmax} = 4. It should be noted that non-scan cells are not clocked while shifting out test responses which leads to zero value in *NT C*.

The Influence of Test Vector and Scan Cell Ordering on Power Minimisation in Full Scan Sequential Circuits Previous research has established that the node transition count in full scan sequential circuits depends on two factors, test vector ordering and scan cell ordering, when the circuit is in the test mode. The following example shows how test vector and scan cell ordering affect the circuit activity during test application in full scan sequential circuits.[2]

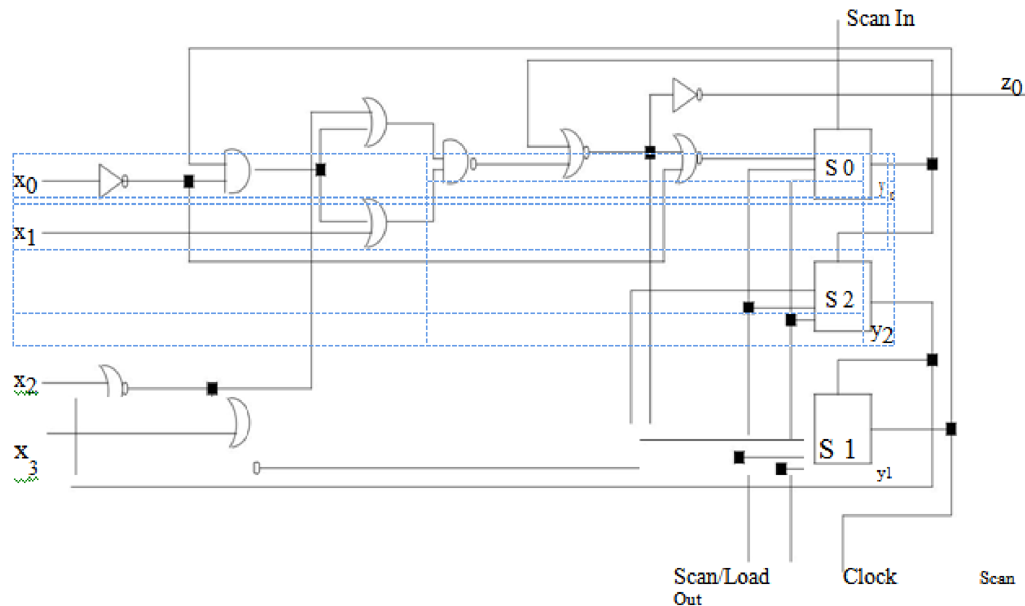


Figure 3: Example 1 circuit after permuting the order of S_1 and S_2

Example 1 To illustrate the factors accountable for power dissipation consider the *s27* circuit (Figure 2) from the commonly accepted ISCAS89 benchmark set. The primary inputs are fx_0;x_1;x_2;x_3g, fS_0;S_1;S_2g are the scan cells, fy_0;y_1;y_2g are the present state lines, and fz_0g is the circuit output. Using the GATEST ATPG tool, it was shown that 5 test vectors are needed to achieve 100% fault coverage. The test vectors are f1101011; 0000000; 0010010; 0111111; 1100010g. For easy reference they are labelled as fV_0;V_1;V_2;V_3;V_4g. Each test vector consists of primary inputs and pseudo inputs (present state lines) in the following order $x_0x_1x_2x_3y_0y_1y_2$. Assuming that initially all the primary and pseudo inputs are set to 0 and using Equation 2 the node transition count is calculated as *NT C* = 372. A detailed description for calculating *NT C* over the entire test application period is outlined. By reordering the test vectors as such fV_0;V_2;V_4;V_3;V_1g a new lower value for node transition count is obtained *NT C* = 352. This shows that reordering of test vectors reduces power dissipation during test application by increasing the correlation between consecutive test vectors. Note that the *NT C* is computed over the entire test application period of n (m + 1) + m clock cycles, where n is the number of test vectors and m is the number of scan cells. Now the effect of scan cell ordering on power savings is examined. Consider the reordered test vector set

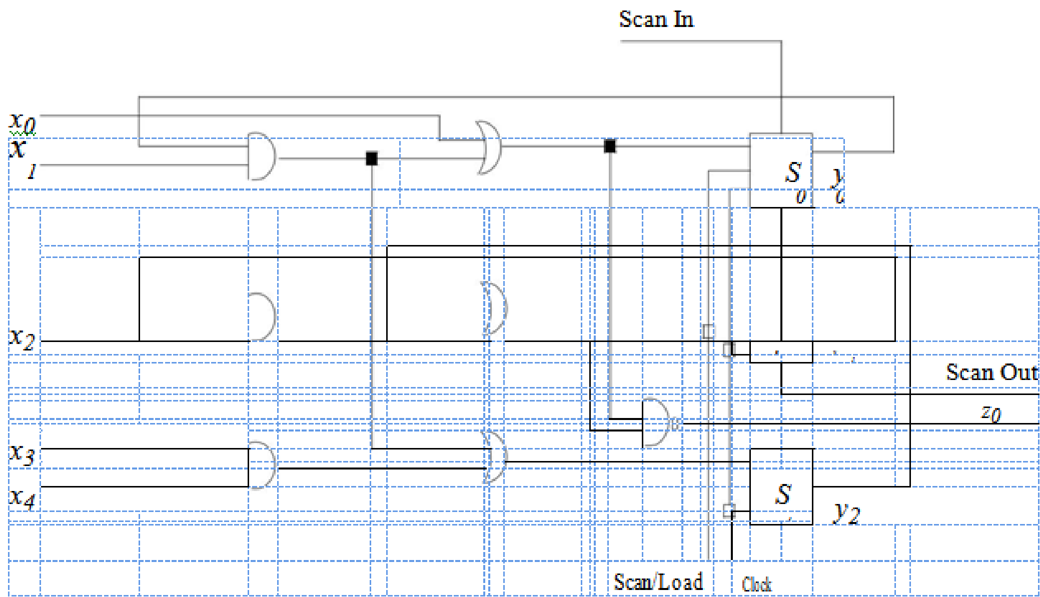


Figure 4: Example 2 partial scan circuit.

fV_0;V_2;V_4;V_3;V_1g and reordering scan cells to fS_0;S_2;S_1g as shown in Figure3 the value of node transition count is reduced further to $NT\ C$ = 328. This reduction is due to the higher correlation between successive states during shifting in test vectors and shifting out test responses. If test vector ordering and scan cell ordering are done simultaneously a further reduction in node transition count is achieved $NT\ C$ = 296, for the following test vector order fV_0;V_2;V_3;V_4;V_1g and scan cell order fS_2;S_1;S_0g. This shows that scan cell ordering and test vector ordering are interrelated which leads to higher savings than when either scan cell ordering or test vector ordering are considered separately.[3]

The Influence of Scan Cell Ordering on Power Minimisation in Partial Scan Sequential Circuits

It was shown in Example 1 how test vector ordering affects circuit activity and hence power dissipation in full scan sequential circuits. However, test vector ordering proposed in prohibited for partial scan due to the fixed test vector order fault activation and fault-effect propagation sequences through non-scan cells. On the other hand, scan cell ordering can be applied for partial scan sequential circuits as shown in the following example.

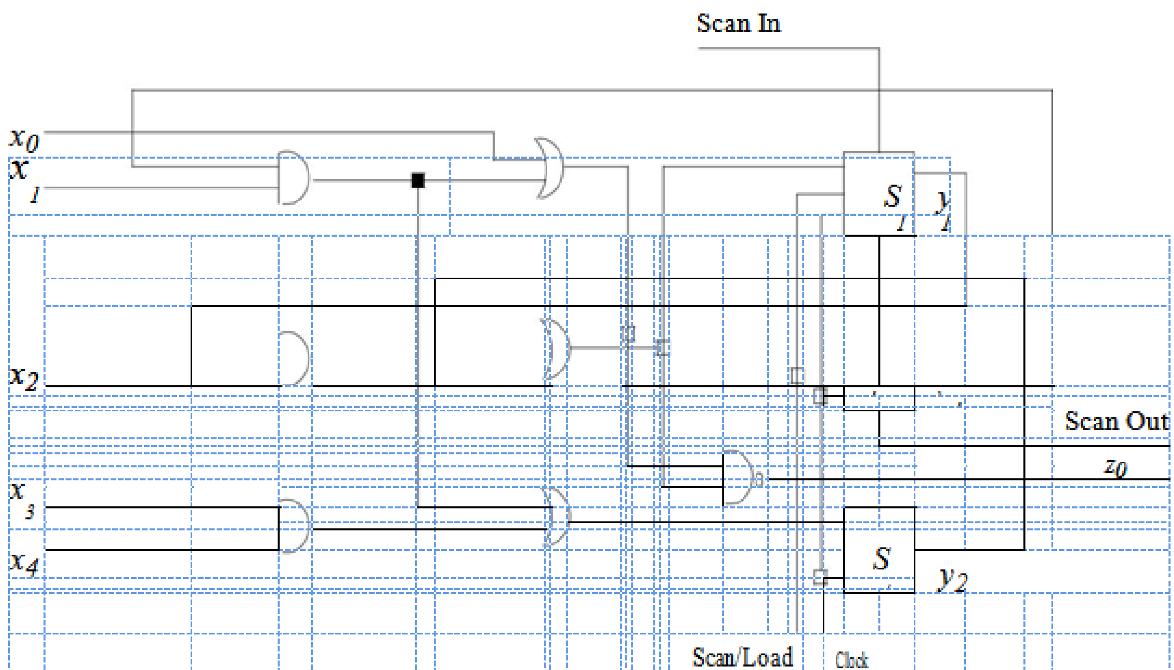


Figure 5: Example 2 partial scan circuit after permuting scan cells S_0 and S_1.

Example 2: To investigate the influence of scan cell ordering on power dissipation during test application in partial scan sequential circuits consider the simple circuit shown in Figure 4. The primary inputs are fx_0;x_1;x_2;x_3;x_4g, fS_0;S_1g are the scan cells, fS_2g is the non-scan cell, fy_0;y_1;y_2g are the present state lines, and fz_0g is the circuit output. The scan cells are selected using the logic level partial scan tool OPUS. Using the logic level ATPG tool GATEST, 6 test vectors are generated to achieve 100% fault coverage. The test vectors are f1011110;0001010;0111010;0110100;1010111;0100101g. For easy reference they are labelled as fV_0;V_1;V_2;V_3;V_4;V_5g. Each test vector consists of a primary input part and a present state part in the following order $x_0x_1x_2x_3x_4y_0y_1$. Initially all the primary inputs and present state lines are considered 0 and using the node transition count is calculated as $NT\ C = 224$. By reordering the scan cells to fS_1;S_0g as shown in Figure 5 the value of the node transition count is reduced to
$NT\ C = 216$.

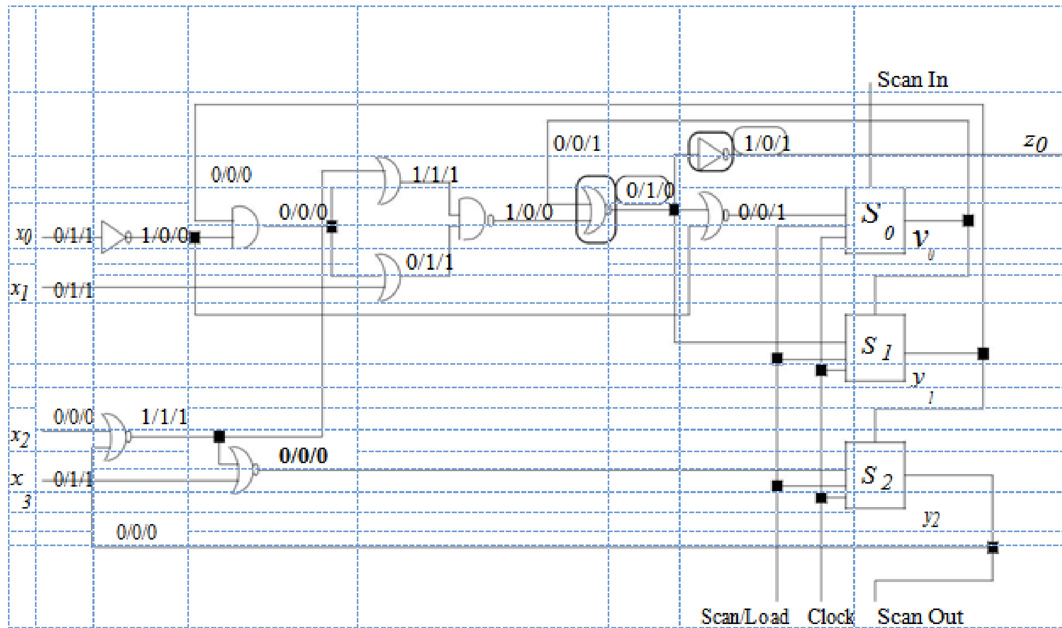
The techniques shown in the previous Examples 1 and 2 yield modest savings in *NT C*, and hence in power dissipation.[4] To further reduce power dissipation during test application in the circuit under test, a new test application strategy is described in the following.

New Technique for Minimisation of Power Dissipation During Test Application By Controlling Primary Input Change Time

In this section the key ideas of the proposed technique are presented. The influence of primary input change time on the reduction of spurious transitions, and hence savings in the total number of transitions, is demonstrated through detailed examples. It introduces the new test application strategy for small to medium sized full scan sequential circuits with no penalty in test area, performance, test efficiency, test application time or volume of test data. illustrates the applicability of the proposed test application strategy to partial scan sequential circuits, and describes how the proposed new test application strategy can be extended to scan BIST methodology introduced in Figure 5

New Test Application Strategy for Full Scan Sequential Circuits

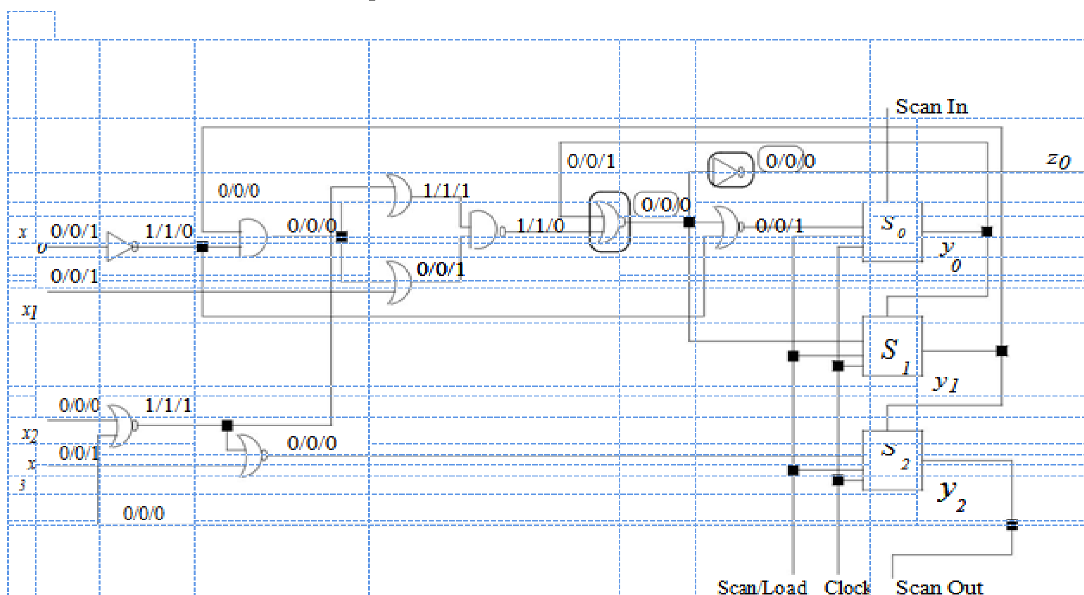
To motivate the need for a new test application strategy for power minimisation, an overview of testing scan sequential circuits is provided. For a scan sequential circuit, each test vector $V_i = x_i@y_i$ applied to the circuit under test is composed of primary input part x_i and pseudo input (present state part) y_i, where @ denotes concatenation. Given m scan cells, for each test vector $V_i = x_i@y_i$ the present state part y_i is shifted in m clock cycles t_0 to $t_{m\ 1}$. In the case of partial scan sequential circuits, the non-scan cells preserve their value during clock cycles t_0 to $t_{m\ 1}$. In the next clock cycle t_m the entire test vector $V_i = x_i@y_i$ is applied to the circuit under test. A scan cycle represents the $m + 1$ clock cycles t_0 to t_m required to shift in the present state part of the test vector and apply the entire test vector to
the circuit under test.[6] In the following m clock cycles of the next scan cycle the test response $y^0{}_{\mathrm{i}}$
is shifted out simultaneously with shifting in the present state part of the next test vector $V_j = x_j @y_j$. The values of the primary inputs are important only at t_m when the entire test vector is applied. Therefore the primary inputs can be changed at clock cycles t_0 to $t_{m\ 1}$without affecting test efficiency.[5] The transitions which occur in the circuit combinational part, without any influence on test efficiency or test data, are defined as follows.



(a) Primary inputs change as soon as possible (ASAP) at t_0

Figure 6: Example circuit illustrating factors which lead to spurious transitions during test application

Definition 1 A spurious transition during test application in scan sequential circuits is a transition which occurs in the combinational part of the circuit under test while shifting out the test response and shifting in the present state part of the next test vector. These transitions do not have any influence on test efficiency since the values at the input and output of the combinational part are not useful test data.
It was assumed in Example1 circuit that changing of the primary inputs $x_0x_1x_2x_3$ occurs at timet_0 The following two definitions introduce two test application strategies that will be used throughout this dissertation.[7]
Definition 2 The test application strategy where primary inputs change is called as soon as possible(ASAP). Definition 3 The test application strategy where primary inputs change that is called m as late as possible (ALAP), where m is the number of sequential elements converted to scan cells.



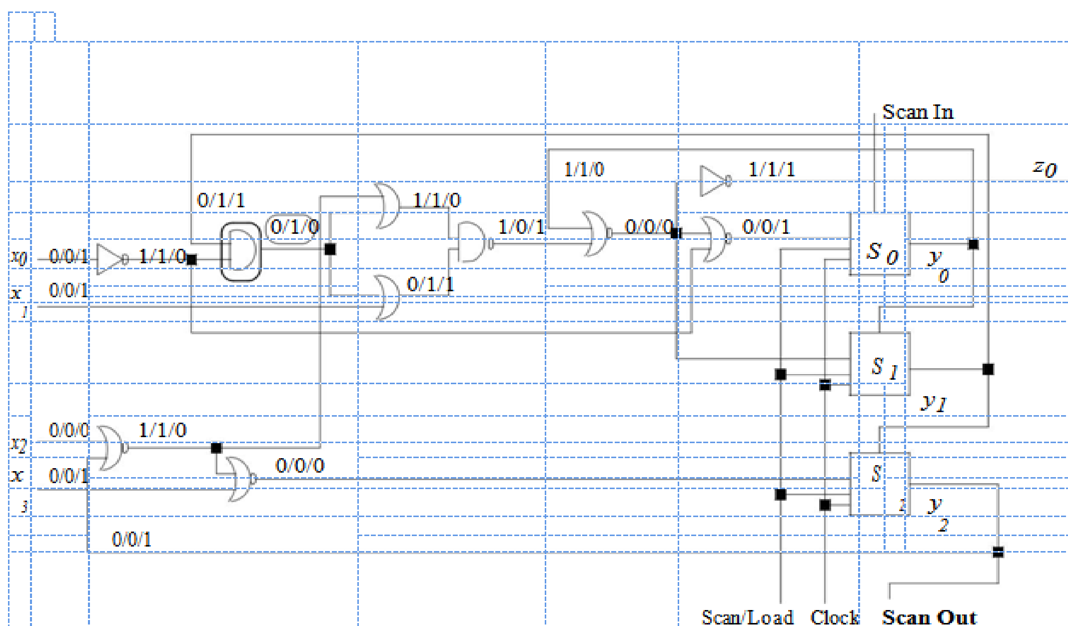
(b) Primary inputs change at t_1

Figure 7: Example circuit illustrating factors which lead to spurious transitions during test application
Having introduced ASAP and ALAP test application strategies the following example shows their shortcomings and the need of a new test application strategy.

Example 3 For the particular example in Figure7, where the number of scan cells is 3, at timest_0, t_1, and t_2 the scan cells are in the shift mode and the values on the input lines of the combinational part of the circuit are irrelevant. The value of primary inputs is important only at$_3$ when the entire test vector is applied to the combinational part of the circuit. Therefore, the primary inputs can keep the value of the previous test vector duringt_0, t_1, andt_2 without affecting the testing process.[8] To illustrate the importance of primary input change time consider the application of test vectorf0000000 g followed by test vectorf1101011g. The circuit lines are described in terms of three values. F example in Figure7(a), in the case of primaryxinput$_0$thevalue=1=10 denotes value 0

f0000000 g and value 1$t_0$atandt when shifting in the second test
att$_3$ when applying

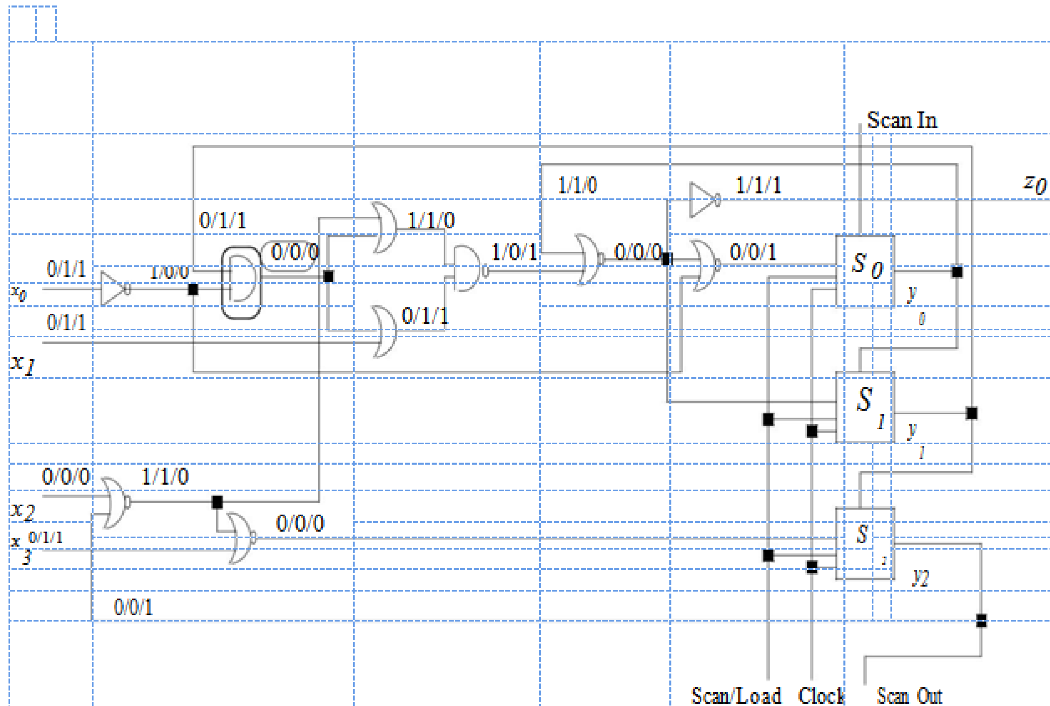
vectorf1101011g. When primary inputsx_0 $x_1x_2x_3$ change att$_0$ (ASAP test application strategy introduced in De nition3 as shown in Figure6(a)the two marked boxes



(c) Primary inputs change as late as possible (ALAP) at t_3

Figure 8: Example circuit illustrating factors which lead to spurious transitions during test application

Illustrate spurious transitions 0=1=0 and 1=0=1 at the output of the marked NOR and NOT gate respectively. Since the value of primary inputs is irrelevant during shifting out the test response, if the primary inputs are changed the at controlling value 1 at the input of the marked NOR gate is preservedt_1 at and no spurious transitions at the output of the marked NOR and NOT gates will occur,[9] as shown in Figure7.The primary inputs can keep their value until when test vectorf1101011g is applied to the circuit (ALAP test application strategy introduced in. definition However, changing the primary inputs at will not yield the minimum number of transitions as demonstrated in Figure8(c)and8(d)using the same test vectors. In Figure.8(c),in the case of primary input x_0 the value=0=1 denotes value 0 at$_1$ andt$_2$ when shifting inf1101011g and value 1 at t when applyingf1101011g. When primary inputsx x x x are changed at as shown 3 0 1 2 3 3 in Figure8 (c)the marked box illustrates a spurious transition=1=0atthe 0output of the marked AND gate. However if the primary inputs are changed earlier the controlling value 0 at the input of the marked AND gate is preserved no spurious transitions at the output of the marked AND gate will occur as shown in Figure8 (d).



(d) Primary inputs change at t_2

Figure 9: Example circuit illustrating factors which lead to spurious transitions during test application

So far it was shown in Example 3 that both ASAP or ALAP test application strategies lead to spurious transitions during shifting in test vectors and shifting out test responses. Now the question is when should the primary inputs change such that the smallest number of spurious transitions occur which leads to lower power dissipation? Before introducing the new test application strategy which reduces spurious transitions during test application the following necessary definition is given.

Definition 4 The best primary input change time of test vector V_j is the time when the primary input part x_i of the previous test vector V_i changes to the primary input part x_j of the actual test vector V_j, leading to the smallest value of node transition count during the scan cycle when test vector V_j is applied after test vector V_i.[10]

Finding the best primary input change time will lead to higher correlation between consecutive values on the input lines of the combinational part of the circuit. This leads to minimum value of NT C during the scan cycle, and yields savings in power dissipation. Definition 5 is used to introduce the new test application strategy.

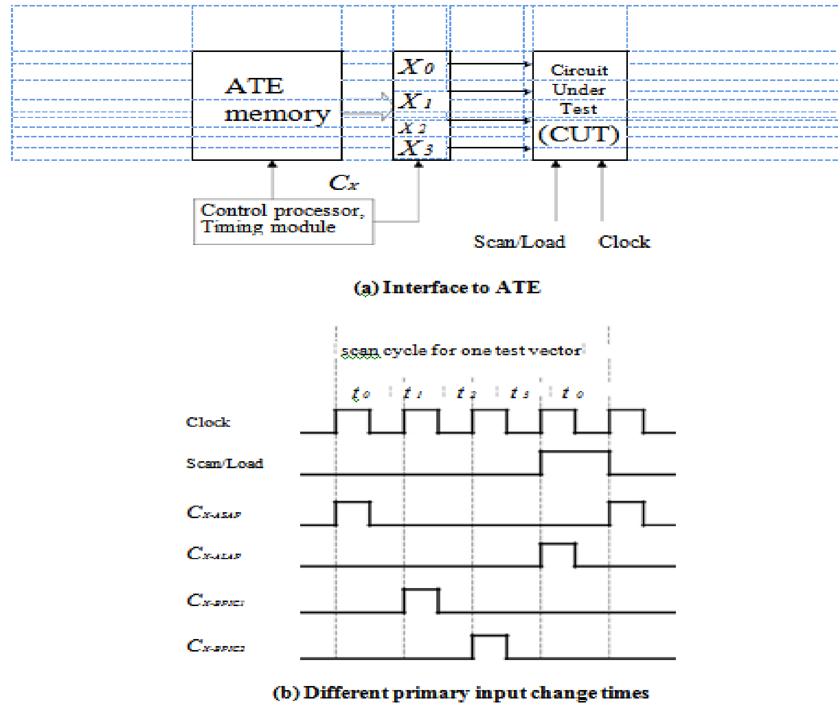


Figure 10: Interface to ATE for different test application strategies.

Definition 5 The test application strategy where best primary input change time for each test vector V_i, with i = 0: : :n 1, is determined such that the minimum value of node transition count over the entire test application period is achieved, is referred to as *best primary input change* (BPIC) test application strategy.

To clarify the notation used throughout this chapter, Figure 10 shows how different test application strategies are interfaced to ATE (Figure 2) under the zero delay models. The control processor and the timing module initialise the primary input values $x_0x_1x_2x_3$ using the C_X signal, as shown in Figure10(a)

Cycle	Vector	Op	SI	x_0	x_1	x_2	x_3	y_2^0	y_1^0	y_0^0	NTC
0 (t_0)	V_0	S	0	1	1	0	1	0	0	0	14
1 (t_1)	V_0	S	1	1	1	0	1	1	0	0	10
2 (t_2)	V_0	S	1	1	1	0	1	1	1	0	19
3 (t_3)	V_0	L	-	1	1	0	1	0	0	1	18
4 (t_0)	V_2	S	0	0	0	1	0	0	0	0	15
5 (t_1)	V_2	S	1	0	0	1	0	1	0	0	10
6 (t_2)	V_2	S	0	0	0	1	0	0	1	0	14
7 (t_3)	V_2	L	-	0	0	1	0	1	1	0	19
8 (t_0)	V_3	S	1	0	1	1	1	1	1	1	11
9 (t_1)	V_3	S	1	0	1	1	1	1	1	1	10
10 (t_2)	V_3	S	1	0	1	1	1	1	1	1	6
11 (t_3)	V_3	L	-	0	1	1	1	0	0	0	18
12 (t_0)	V_4	S	0	1	1	0	0	0	0	0	16
13 (t_1)	V_4	S	1	1	1	0	0	1	0	0	10
14 (t_2)	V_4	S	0	1	1	0	0	0	1	0	24
15 (t_3)	V_4	L	-	1	1	0	0	0	1	0	16
16 (t_0)	V_1	S	0	0	0	0	0	0	0	1	18
17 (t_1)	V_1	S	0	0	0	0	0	0	0	0	18
18 (t_2)	V_1	S	0	0	0	0	0	0	0	0	6
19 (t_3)	V_1	L	-	0	0	0	0	0	0	0	6
20 (t_0)	-	S	0	0	0	0	0	0	0	0	6
21 (t_1)	-	S	0	0	0	0	0	0	0	0	6
22 (t_2)	-	S	0	0	0	0	0	0	0	0	6
				TOTAL							296

(a) As Soon As Possible (ASAP) test application strategy

Table 1: The flow of test data for the circuit in Figure 6 during the entire test application period

Depending on the value of the Scan/Load signal, different primary input change times are chosen by the activation of C_X , as illustrated in Figure 10(b). For example, in the case of the ASAP test application strategy, $C_{X\ \mathrm{ASAP}}$is active only at t_0. Similarly, the primary inputs change at t_1 by the activation of $C_{X\ \mathrm{BPIC1}}$at t_1.

Figures 9(a) to 9(d) have illustrated the reduction of spurious transitions over a three clock cycle's period. The following example gives insight of the proposed technique for power dissipation minimisation during the entire test application period when applied to full scan sequential circuits.

Cycle	Vector	Op	SI	x_0	x_1	x_2	x_3	y_2^0	y_1^U	y_0^U	NTC
0 (t_0)	V_0	S	0	0	0	0	0	0	0	0	6
1 (t_1)	V_0	S	1	0	0	0	0	1	0	0	10
2 (t_2)	V_0	S	1	**1**	**1**	**0**	**1**	1	1	0	17
3 (t_3)	V_0	L	-	1	1	0	1	0	0	1	18
4 (t_0)	V_2	S	0	**0**	**0**	**1**	**0**	0	0	0	15
5 (t_1)	V_2	S	1	0	0	1	0	1	0	0	10
6 (t_2)	V_2	S	0	0	0	1	0	0	1	0	14
7 (t_3)	V_2	L	-	0	0	1	0	1	1	0	19
8 (t_0)	V_3	S	1	**0**	**1**	**1**	**1**	1	1	1	11
9 (t_1)	V_3	S	1	0	1	1	1	1	1	1	10
10 (t_2)	V_3	S	1	0	1	1	1	1	1	1	6
11 (t_3)	V_3	L	-	0	1	1	1	0	0	0	18
12 (t_0)	V_4	S	0	0	1	1	1	0	0	0	10
13 (t_1)	V_4	S	1	0	1	1	1	1	0	0	10
14 (t_2)	V_4	S	0	0	1	1	1	0	1	0	14
15 (t_3)	V_4	L	-	**1**	**1**	**0**	**0**	0	1	0	16
16 (t_0)	V_1	S	0	1	1	0	0	0	0	1	14
17 (t_1)	V_1	S	0	**0**	**0**	**0**	**0**	0	0	0	18
18 (t_2)	V_1	S	0	0	0	0	0	0	0	0	6
19 (t_3)	V_1	L	-	0	0	0	0	0	0	0	6
20 (t_0)	-	S	0	0	0	0	0	0	0	0	6
21 (t_1)	-	S	0	0	0	0	0	0	0	0	6
22 (t_2)	-	S	0	0	0	0	0	0	0	0	6
				TOTAL							266

(b) Proposed Best Primary Input Change (BPIC) test application strategy

Table 2: The flow of test data for the circuit in Figure 6 during the entire test application period

Example 4 Tables 1(a) and 1(b) show the flow of test data for the benchmark circuit *s27* of Figure 9 for ASAP and the proposed test application strategy respectively.[11] In Table 1(a) consider the scan cell order f S_2;S_1;S_0g and test vector order f V_0;V_2;V_3;V_4;V_1g after simultaneous test vector ordering and scan cell ordering was carried out as shown in t. Column shows the clock cycle index and the second column outlines the test vector which is scanned in during t_0, t_1, t_2 and applied at t_3. The operation type

Cycle	Vector	Op	SI	x_0	x_1	x_2	x_3	y_1^U	y_2^0	y_0^U	NTC
0 (t_0)	V_1	S	0	**0**	**0**	**0**	**0**	0	0	0	6
1 (t_1)	V_1	S	0	0	0	0	0	0	0	0	6
2 (t_2)	V_1	S	0	0	0	0	0	0	0	0	6
3 (t_3)	V_1	L	-	0	0	0	0	0	0	0	6
4 (t_0)	V_0	S	0	**1**	**1**	**0**	**1**	0	0	0	14
5 (t_1)	V_0	S	1	1	1	0	1	1	0	0	10
6 (t_2)	V_0	S	1	1	1	0	1	1	1	0	10
7 (t_3)	V_0	L	-	1	1	0	1	0	0	1	27
8 (t_0)	V_4	S	0	1	1	0	1	0	0	0	14
9 (t_1)	V_4	S	0	**1**	**1**	**0**	**0**	0	0	0	11
10 (t_2)	V_4	S	1	1	1	0	0	1	0	0	10
11 (t_3)	V_4	L	-	1	1	0	0	1	0	0	6
12 (t_0)	V_3	S	1	1	1	0	0	1	1	0	10
13 (t_1)	V_3	S	1	**0**	**1**	**1**	**1**	1	1	1	16
14 (t_2)	V_3	S	1	0	1	1	1	1	1	1	10
15 (t_3)	V_3	L	-	0	1	1	1	0	0	0	18
16 (t_0)	V_2	S	0	0	1	1	1	0	0	0	10
17 (t_1)	V_2	S	0	0	1	1	1	0	0	0	6
18 (t_2)	V_2	S	1	0	1	1	1	1	0	0	10
19 (t_3)	V_2	L	-	**0**	**0**	**1**	**0**	1	1	0	19
20 (t_0)	-	S	1	0	0	1	0	1	1	1	10
21 (t_1)	-	S	1	0	0	1	0	1	1	1	10
22 (t_2)	-	S	1	0	0	1	0	1	1	1	6
				TOTAL							251

(c) Proposed Best Primary Input Change (BPIC) test application strategy combined with simultaneous scan cell and test vector ordering

Table 3: The flow of test data for the circuit in Figure 6 during the entire test application period

(Scan or Load) is shown in column 3. In the case of a Scan operation the fourth column gives the *Scan In* value. Columns 5-8 show the values of primary inputs $x_0x_1x_2x_3$ and the columns 9-11 show the next state values y^0 y^0 y^0 The last column shows the value of the 2 1 0 node transition count *NT C* for each clock cycle. The *NT C* is calculated as follows. In clock cycle (*i*) the *NT C* in the combinational part is computed by considering the primary inputs of clock cycle (*i*) and the next state values of clock cycle (*i* 1), which are present state values at clock cycle (*i*). The *NT C* in the sequential part is the sum of *NT C* of each

2 1 0 in clock cycle (

scan cell by scanning/loading the next state values y^0 y^0 y^0 *i), using the*

values of N_{SCmin} and N_{SCmax} outlined. Initially all the primary and scan in-puts are set to 0 and the node transition count over the entire test application period under the ASAP test application strategy is NT C = 296. This value can be reduced if spurious transitions during shifting in test vectors and shifting out responses are avoided by modifying the primary input change time. The change of primary input part of test vector V_i at time t $_j$ is indicated by $t_{Vi} = t_j$. If the primary input change times are set to $t_{V0} = t_2$, $t_{V2} = t_0$, $t_{V3} = t_0$, $t_{V4} = t_3$, and $t_{V1} = t_1$ as shown in the marked boxes of Table 1(b), the node transition count reduces to NT C = 266. The reason for reducing the number of transitions is the increased correlation between consecutive values of primary and pseudo inputs duringt_0, t_1, t_2, when test vectors are scanned in and test responses are scanned out. For example by changing the primary inputs of t_{V4} at t_3 the NT C in clock cycles 12 and 14 reduces from 16 and 24 respectively in the case of ASAP (Table 1(a)) to 10 and 14 respectively in the case of BPIC (Table 1(b)). Note that in clock cycles when test responses are loaded in scan cells (L in column 3), the correct test response values from Table 1(a) are preserved. When combining primary input change time with simultaneous scan cell ordering and test vector ordering further improvements are achieved. For test vector order f V_1;V_0;V_4;V_3;V_2g, scan cell order f S_1;S_2;S_0g and primary input change times set at $t_{V1} = t_0$, $t_{V0} = t_0$, $t_{V4} = t_1$, $t_{V3} = t_1$, and $t_{V2} = t_3$, it is shown that the new value of node transition count is reduced further to NT C = 251 (Table1(c)). This highlight the importance of combining the best primary input change time with simultaneous scan cell and test vector ordering forNT C reduction.

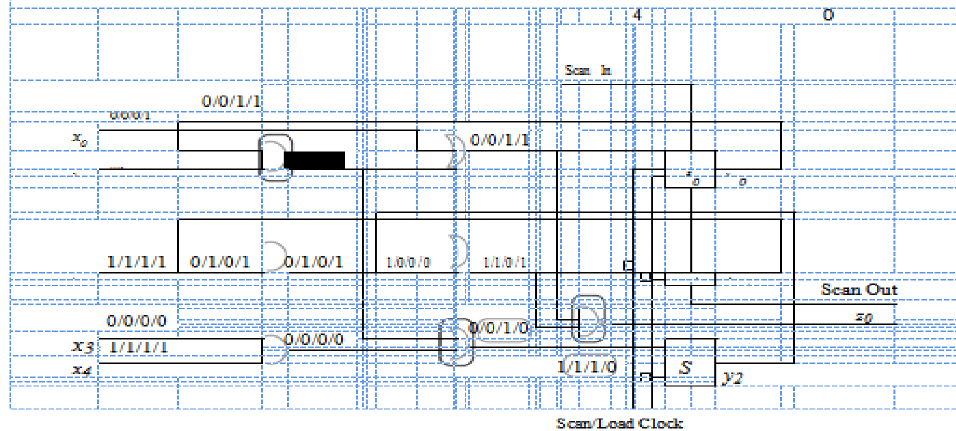
Summary: The previous Example 4 has highlighted the importance of combining primary input change time with scan cell and test vector ordering*NT*for*C*
reduction in full scan sequential circuits. In the case of the ASAP test application strategy, the node transition count is NT C = 296 over the entire test application period (Table1(a)). When applying the proposed BPIC test application strategy node transition count is reduced to *NT C* = 266 (Table1(b)). To achieve maximum reduction in node transition count, the proposed BPIC test application strategy is combined with scan cell and test vector ordering leading to *NT C* = 251 (Table1(c)). Computing the best primary input change time for every test vector is described in the algorithm *BPIC-ALG.*

The Applicability of the New Test Application Strategy to Partial Scan Sequential Circuits

Having introduced the new BPIC test application strategy for full scan sequential circuits, this section shows through two detailed examples that the BPIC test application strategy is applicable to partial scan sequential circuits. The importance of combining the proposed test application strategy with scan cell ordering is outlined.

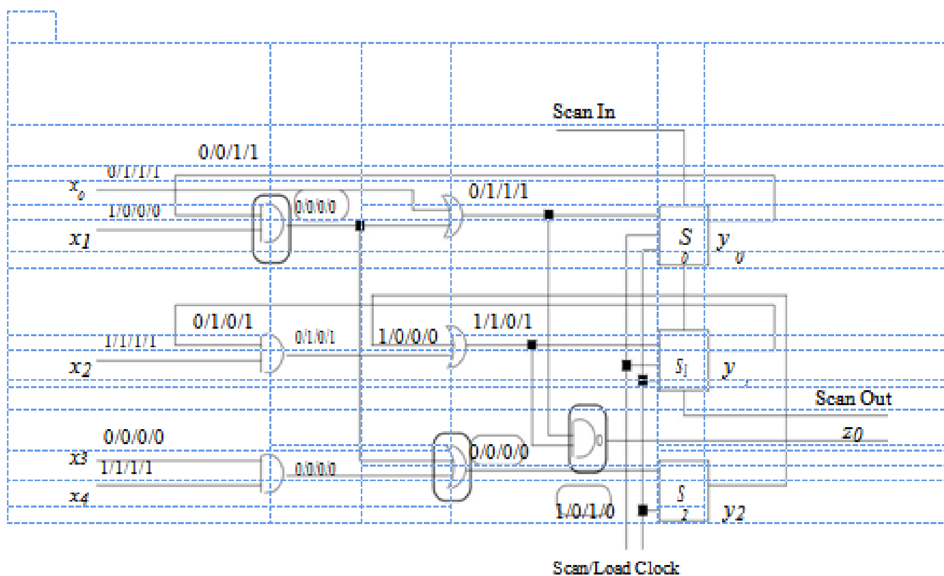
So far it was assumed that the changing time of the primary inputs $x_0x_1x_2x_3x_4$ of circuit shown in Figure 4 (Example 2) occurs at clock cycle t_2. To illustrate the importance of primary input change time on the number of spurious transitions in partial scan sequential circuits consider the following example.[12]

Example 5 Consider the application of test vectorV_3=f0110100g followed by test vectorV_4=f1010111g to the circuit of Figure.8 The circuit data lines are described in terms of four values. For example in 3Figure.8(a),in the case of primary xinput$_0$thevalue 0 =0=0=1 denotes value 0 at$_2$ when applyingV_3, value 0 att$_0$ andt$_1$ respectively when shifting in the present state part of the second test V vector, and value 1 at when applying V_4.



(a) Primary inputs change as late as possible (ALAP)t at

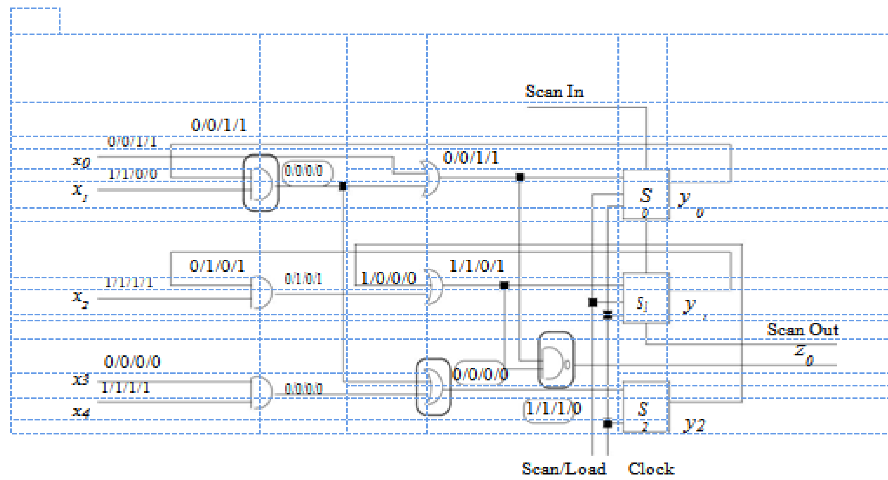
Figure 11: Example partial scan sequential circuit illustrating the effect of primary input change time on the reduction of spurious transitions during test application



(b) Primary inputs change as soon as possible (ASAP) at t_0

Figure 12: Example partial scan sequential circuit illustrating the effect of primary input change time on the reduction of spurious transitions during test application

When primary inputs $x_0x_1x_2x_3x_4$ change at t_2 as shown in Figure 12(a) the two marked boxes illustrate the spurious transition 0=0=1=0 at the output of the marked AND gate which further propagates at the output of the marked OR gate. However the value of primary inputs is irrelevant during shifting out the test response. Thus, the primary inputs can be changed as early tasafter test vector V is applied to the circuit under test. When primary inputs$x_0x_1x_2x_3x_4$ change att$_0$ as shown in Figure11(b)the controlling value 0 at the input of the marked AND gate is preserved no spurious transitions at the output of the marked AND and OR gates will occur. However, changing the primary inputs at does not yield the minimum value of node transition count. The marked box in Figure11(b)illustrates a spurious transition=0=1=0 at the output of the marked NAND gate. The value of NTC= 41 over the scan cycle periodt$_0$, t$_1$ andt$_2$ in the case of ALAP test application strategy is reduced NTC=to 37 in the case ASAP test application strategy. However, both ALAP and ASAP test application strategies fail to achieve the minimum NTC. If the primary inputs change at clock cyclet$_1$ the controlling value 0 at the input of the marked NAND gate is preservedt$_0$atand no spurious transitions at the output of the marked NAND gate will occur, as shown in Figure6(c). Furthermore, the



(c) Primary inputs change at t_1

Figure 8: Example partial scan sequential circuit illustrating the effect of primary input change time on the reduction of spurious transitions during test application controlling value 0 at the input of the marked AND gate is preserved at t_1 and no spurious transitions at the output of the marked AND and OR gates will occur, as shown in the marked boxes in Figure 11(c). Thus, the minimum value of NT C = 35 is achieved when primary input change time is set t_1o. Figures11(a)-`11(c) have illustrated the reduction of spurious transitions during a four clock cycles period. Now, to give insight of the proposed BPIC test application strategy during the entire test application period in partial sequential circuits, consider the following example.

Example 6 To outline the advantage of controlling primary input change time of each test vector, Tables2(a) and11(b) show the flow of test data for the circuit of Figure 11 for ALAP and BPIC test application strategy respectively, during the entire test application period. The first column shows the clock cycle index and the second column outlines the test vector which is scanned in duringt_0, t_1 and applied at$_2$. The operation type Scan(or Load) is shown in the third column. In the case of Scan operation the fourth column gives the value on scan input line Scan In. Columns 5-9 show the values of primary inputs

Cycle	Vector	Op	SI	x_0	x_1	x_2	x_3	x_4	y_0^U	y_1^U	y_2^U	NTC
0 (t_0)	V_0	S	0	0	0	0	0	0	0	0	0	4
1 (t_1)	V_0	S	1	0	0	0	0	0	1	0	0	8
2 (t_2)	V_0	L	-	1	0	1	1	1	1	0	1	12
3 (t_0)	V_1	S	0	1	0	1	1	1	0	1	1	15
4 (t_1)	V_1	S	1	1	0	1	1	1	1	0	1	13
5 (t_2)	V_1	L	-	0	0	0	1	0	0	1	0	22
6 (t_0)	V_2	S	0	0	0	0	1	0	0	0	0	10
7 (t_1)	V_2	S	1	0	0	0	1	0	1	0	0	8
8 (t_2)	V_2	L	-	0	1	1	1	0	1	0	1	13
9 (t_0)	V_3	S	0	0	1	1	1	0	0	1	1	15
10 (t_1)	V_3	S	0	0	1	1	1	0	0	0	1	15
11 (t_2)	V_3	L	-	0	1	1	0	1	0	1	0	13
12 (t_0)	V_4	S	1	0	1	1	0	1	1	0	0	13
13 (t_1)	V_4	S	1	0	1	1	0	1	1	1	0	16
14 (t_2)	V_4	L	-	1	0	1	0	1	1	1	0	12
15 (t_0)	V_5	S	1	1	0	1	0	1	1	1	0	4
16 (t_1)	V_5	S	0	1	0	1	0	1	0	1	0	8
17 (t_2)	V_5	L	-	0	1	0	0	1	0	0	0	15
18 (t_0)	-	S	0	0	1	0	0	1	0	0	0	4
19 (t_1)	-	S	0	0	1	0	0	1	0	0	0	4
				TOTAL								224

(a) As Late As Possible (ALAP) test application strategy

Table 4: Flow of test data for the circuit in Figure 8 during the entire test application period for ALAP and BPIC test application strategies and its effect on *NT C*

x0x1x2x3x4 and the columns 10-12 show the next state values *y*0 *y*0 *y*0 . The last column 0 1 2 13 shows the value of *NT C* for each clock cycle. The *NT C* is calculated as follows. In clock cycle (*i*) the *NT C* in the combinational part is computed by considering the primary inputs of clock cycle (*i*) and the next state values at clock cycle (*i* 1), which are present state values at clock cycle (*i*). The *NT C* in the sequential part is the sum of *NT C* of each cell (scan cells S_0 and S_1 and non-scan cell S_2) by scanning/loading the next state

values y^0_0 $y^0_1 y^0_2$ in clock cycle (*i*), using the values of N_{SCmin} , N_{SCmax} , N_{NSCmin} , and N_{NSCmax}

Outlined. Note that when shifting out test responses the non-scan cell S_2 is not clocked and therefore no transitions occur.[13] Initially all the primary inputs and present state lines are considered 0 and the node transition count over the entire test application

Cycle	Vector	Op	SI	x_0	x_1	x_2	x_3	x_4	y_0^0	y_1^0	y_2^0	NTC
0 (t_0)	V_0	S	0	1	0	1	1	1	0	0	0	8
1 (t_1)	V_0	S	1	1	0	1	1	1	1	0	0	8
2 (t_2)	V_0	L	-	1	0	1	1	1	1	0	1	8
3 (t_0)	V_1	S	0	0	0	0	1	0	0	1	1	18
4 (t_1)	V_1	S	1	0	0	0	1	0	1	0	1	12
5 (t_2)	V_1	L	-	0	0	0	1	0	0	1	0	16
6 (t_0)	V_2	S	0	0	0	0	1	0	0	0	0	10
7 (t_1)	V_2	S	1	0	1	1	1	0	1	0	0	8
8 (t_2)	V_2	L	-	0	1	1	1	0	1	0	1	13
9 (t_0)	V_3	S	0	0	1	1	0	1	0	1	1	15
10 (t_1)	V_3	S	0	0	1	1	0	1	0	0	1	15
11 (t_2)	V_3	L	-	0	1	1	0	1	0	1	0	13
12 (t_0)	V_4	S	1	0	1	1	0	1	1	0	0	13
13 (t_1)	V_4	S	1	1	0	1	0	1	1	1	0	13
14 (t_2)	V_4	L	-	1	0	1	0	1	1	1	0	9
15 (t_0)	V_5	S	1	1	0	1	0	1	1	1	0	4
16 (t_1)	V_5	S	0	1	0	1	0	1	0	1	0	8
17 (t_2)	V_5	L	-	0	1	0	0	1	0	0	0	15
18 (t_0)	-	S	0	0	1	0	0	1	0	0	0	4
19 (t_1)	-	S	0	0	1	0	0	1	0	0	0	4
				TOTAL								214

(b) Proposed Best Primary Input Change (BPIC) test application strategy

Table 4: Flow of test data for the circuit in Figure 8 during the entire test application period for ALAP and BPIC test application strategies and its effect *NT* on *C*

period under the ALAP test application strategy is NT C = 224. This value can be reduced if spurious transitions are avoided by determining best primary input change time for each test vector. If the primary input change times are set$_{V0}$to= t_0, $t_{V1} = t_0$, $t_{V2} = t_1$, $t_{V3} = t_0$, $t_{V4} = t_1$, and $t_{V5} = t_2$ as shown in the marked boxes of Table 3(b), the node transition count reduces to NT C = 214. The reason for reducing NT C is the increased correlation between consecutive values of primary inputs and present state lines. For example by changing test vector V_4 at t_1 ($t_{V4} = t_1$) the NT C in clock cycles 13 and 14 reduces from 16 and 12 respectively in the case of ALAP (Table 3(a)) to 13 and 9 respectively in the case of BPIC (Table 4)). It should be noted that for the particular circuit of Figure 8 the value of NT C = 214 when applying the proposed BPIC test application strategy

Cycle	Vector	Op	SI	x_0	x_1	x_2	x_3	x_4	y_1^U	y_0^U	y_2^U	NTC
0 (t_0)	V_0	S	1	0	0	0	0	0	1	0	0	8
1 (t_1)	V_0	S	0	0	0	0	0	0	0	1	0	12
2 (t_2)	V_0	L	-	**1**	**0**	**1**	**1**	**1**	**0**	**1**	**1**	**12**
3 (t_0)	V_1	S	1	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**18**
4 (t_1)	V_1	S	0	0	0	0	1	0	0	1	1	12
5 (t_2)	V_1	L	-	0	0	0	1	0	1	0	0	16
6 (t_0)	V_2	S	1	0	0	0	1	0	1	1	0	10
7 (t_1)	V_2	S	0	0	0	0	1	0	0	1	0	8
8 (t_2)	V_2	L	-	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**13**
9 (t_0)	V_3	S	0	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**11**
10 (t_1)	V_3	S	0	0	1	1	0	1	0	0	1	10
11 (t_2)	V_3	L	-	0	1	1	0	1	1	0	0	12
12 (t_0)	V_4	S	1	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**12**
13 (t_1)	V_4	S	1	1	0	1	0	1	1	1	0	4
14 (t_2)	V_4	L	-	1	0	1	0	1	1	1	0	5
15 (t_0)	V_5	S	0	1	0	1	0	1	0	1	0	8
16 (t_1)	V_5	S	1	1	0	1	0	1	1	0	0	16
17 (t_2)	V_5	L	-	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**11**
18 (t_0)	-	S	0	0	1	0	0	1	0	0	0	4
19 (t_1)	-	S	0	0	1	0	0	1	0	0	0	4
				TOTAL								**206**

(c) Proposed Best Primary Input Change (BPIC) test application strategy combined with scan cell ordering

Table 5: Flow of test data for the circuit in Figure11 during the entire test application period for ALAP and BPIC test application strategies and its effect *NT* on *C*

by itself is better than when applying scan cell ordering by itself (NT C = 216 as shown in Example2). When combining BPIC test application strategy with scan cell ordering further improvements are achieved. For scan cell order f S_1;S_0g and primary input change times set at $t_{V0} = t_2$, $t_{V1} = t_0$, $t_{V2} = t_2$, $t_{V3} = t_0$, $t_{V4} = t_0$, and $t_{V5} = t_2$, it is shown that the new value of node transition count is further reduced to NT C = 206 (Table5(c).

Summary: The previous Example6 has highlighted the importance of combining primary input change time with scan cell ordering for NT C reduction in partial scan sequential circuits. To achieve maximum reduction in node transition count the proposed BPIC test application strategy is combined with scan cell ordering leading to NT C = 206

2(c) from Example 6). Note that the proposed BPIC test application strategy which is equally applicable to both full and partial scan sequential circuits depends only on controlling primary input change time, and hence does not require extra DFT hardware.[14] This means that power dissipation is minimised without an increase in test area or performance. Furthermore, since no extra test data is necessary and the complete test vector computed by the ATPG tool is applied to the circuit under test irrespective of the primary input change time, the proposed test application strategy does not decrease test efficiency and no penalty in test application time or volume of test data is added. Unlike the case of extra primary input vectors, the proposed BPIC test application strategy minimises power dissipation with no penalty in test area, performance, test efficiency, test application time or volume of test data. Furthermore, in the case of the proposed BPIC test application strategy the computational time is low since the algorithm for finding the best primary input change is polynomial and can be used for computing the cost function in the design space exploration as explained.

Extension of the New BPIC Test Application Strategy to Scan BIST Methodology

So far the proposed BPIC test application strategy (Definition 5) was applied to full and partial scan sequential circuits using external automatic test equipment ATE (Figure 1). This can be summarised in Figure 9 where the best primary input change time *k* is highlighted. However, the proposed BPIC test application strategy is not applicable only to standard full and partial scan sequential circuits using external ATE. In the following the minor modifications which need to be considered when using scan BIST methodology (Figure 5) are outlined.

Figure 10 shows that the serial output of the linear feedback shift register (LFSR) is fed directly into the scan chain and the primary inputs are directly controllable. Therefore, primary inputs can be changed at the best primary input change time which is calculated in the same way as for full scan and partial scan sequential circuits as described in the following. This will lead to a lower area overhead associated with scan BIST methodology (Figure 5) at the expense of higher interference from ATE which needs to store the primary input part of each test vector.

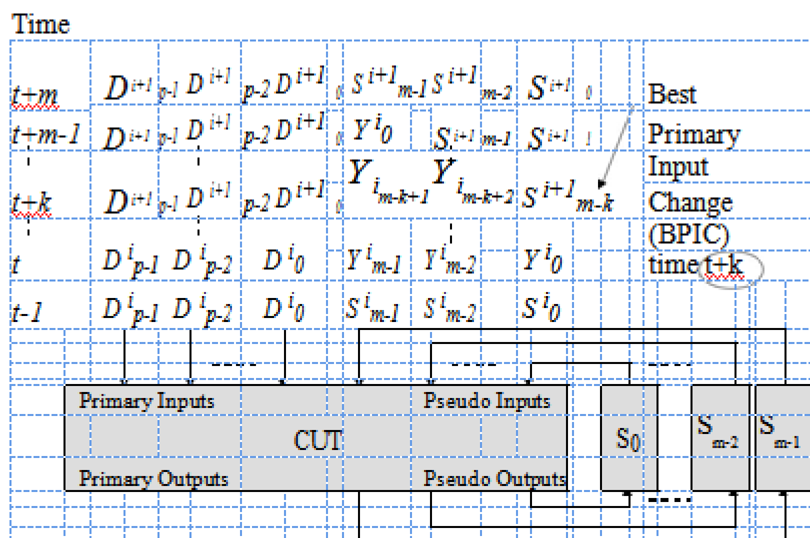


Figure 12: Summary of the proposed BPIC test application strategy when employing standard scan DFT using external ATE

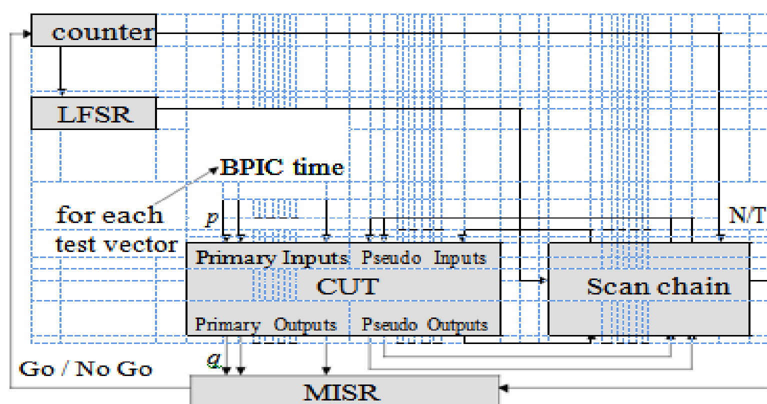


Figure 13: Extension of the proposed BPIC test application strategy to scan BIST methodology

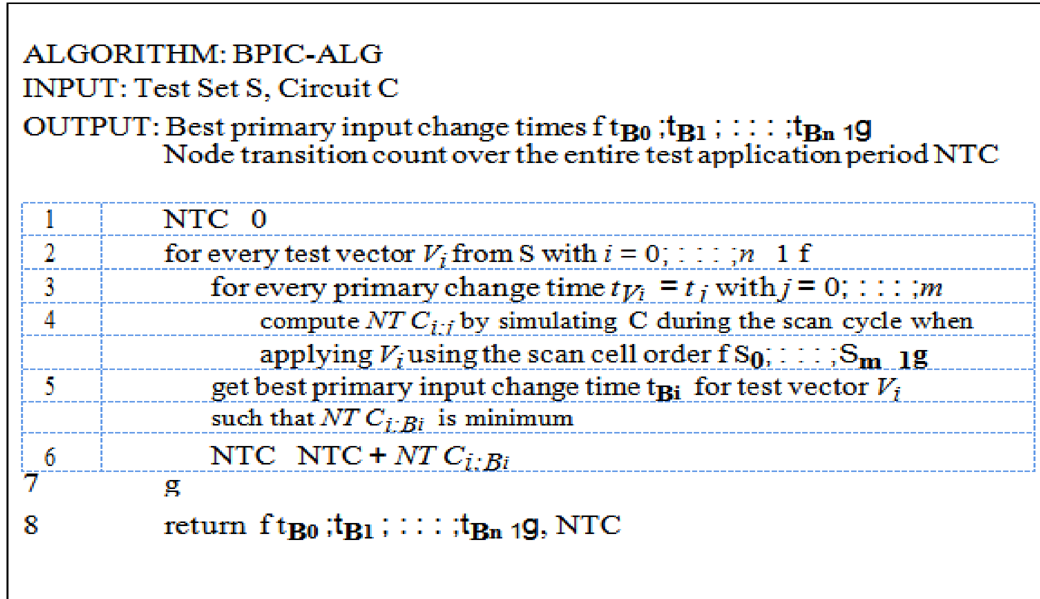
Novel Algorithms for Minimising Power Dissipation during Test Application

Having described in the new best primary input change (BPIC) test application strategy (Definition 5), now algorithms which compute best primary input change times used by BPIC test application strategy are considered.[15] Introduces a new and exact algorithm which computes best primary input change time for each test vector with respect to a given test vector and scan cell order. It shows how combining the proposed test application strategy with the recently introduced scan cell and test vector ordering using a simulated annealing-based design space exploration leads to further reductions in power dissipation during test application.

Best Primary Input Change (*BPIC) Algorithm*

Spurious transitions (Definition 1) induced by fixed primary input changes as outlined in Section 3.3 are solved by changing the primary inputs of each test vector such that the minimum number of transitions is achieved. For a given scan cell order with m scan cells, the total number of primary input change times is $(m + 1)$. Considering n test vectors, in a given test vector order, the total number of configurations of primary input changing for all the test vectors is $(m + 1)^n$. Best Primary Input Change Algorithm (*BPIC-ALG*) computes the best primary input change time for each test vector for a given scan cell order and test vector order. Figure 11 illustrates the pseudo code of the proposed *BPIC-ALG* algorithm. The function accepts as input, a test set S and a circuit C. The outer loop represents the traversal of all the test vectors from test set S. All the $m + 1$ primary input change times for test vector V_i are then considered in the inner loop. For each primary
input change time t_j, circuit C is simulated and the node transition count $NT\ C_{i;\ j}$ is registered. After the completion of the inner loop the best primary input change time t_{Bi}, for which $NT\ C_{i;Bi}$ is minimum, is retained and the outer loop continues until the entire test set is examined. The algorithm computes the best solution in a computational time which is polynomial in the number of test vectors n, the number of scan cells m, and the

circuit size jCj. It should be noted that *BPIC-ALG* is *test set dependent* and hence it is applicable only to *to small to medium sized* sequential circuits as outlined. Despite the reductions which are achieved by the *BPIC-ALG* algorithm as shown in


ALGORITHM: BPIC-ALG
INPUT: Test Set S, Circuit C
OUTPUT: Best primary input change times f t_{B0} ;t_{B1} ; : : : ;t_{Bn} 1g
Node transition count over the entire test application period NTC

1	NTC 0
2	for every test vector V_i from S with i = 0; : : : ;n 1 f
3	for every primary change time t_{Vi} = t_j with j = 0; : : : ;m
4	compute $NTC_{i:j}$ by simulating C during the scan cycle when
	applying V_i using the scan cell order f S_0; : : : ;S_m 1g
5	get best primary input change time t_{Bi} for test vector V_i
	such that $NTC_{i:Bi}$ is minimum
6	NTC NTC + $NTC_{i:Bi}$

7 g

8 return f t_{B0} ;t_{B1} ; : : : ;t_{Bn} 1g, NTC

Figure 13: Proposed *BPIC-ALG* algorithm for determining the Best Primary Input Change time for each test vector

All the factors accountable for power dissipation during test application must be combined for achieving best results, as described in the following section.

Simulated Annealing-Based Design Space Exploration

High power dissipation problems caused by an inadequate test vector ordering and scan cell ordering for full scan sequential circuits are solved by an simulated annealing algorithm which can escape local minima. Since test vector ordering is not applicable to partial scan as outlined. The simulated annealing algorithm for partial scan sequential circuits uses only scans cell ordering. For a test set which consists of n test vectors there are n! test vector orderings. Furthermore for each test vector ordering there are m! scan cell orderings, where m is the number of scan cells. Finding the optimum test vector and scan cell order is NP-hard. The total complexity of the design space, defined by the set of scan cell and test vector orderings, is$n$! Fi m! Which even for small design problems with 15 test vectors and 15 scan cells is computationally expensive.[16] Figure 12 illustrates the basic steps of simulated annealing-based optimisation. The optimisation function accepts as input a test set S and a circuit C which are set to initial configuration S_{INIT} and C_{INIT} respectively. The calculation of the initial control parameter value is based on the assumption that a sufficiently large number of generated solutions (for example 95%) should be accepted at the beginning of the annealing pro-cess. The outer loop modifies the control parameter of the simulated annealing algorithm which is gradually lowered as the annealing process proceeds. Within the inner loop a new sequence of solutions is generated at a constant control parameter value. The length of a sequence of solutions is set to 20. The control parameter is decreased in such a way that the stationary distributions at the end of the sequences of solutions are close to each other. By evaluating information about the cost distribution within each sequence of solutions, a fast decrease of the control parameter is given according to the cooling schedule from. Each new solution is generated using one of the following:

ž randomly choose two scan cells S_i and S_j from the actual scan cell order f S_0; : : : ;S_i;

: : : ;S_j ; : : : ;$S_{m\ 1}$g and exchange their position generating a new scan cell order

f S_0; : : : ;S_j ; : : : ;S_i; : : : ;$S_{m\ 1}$g, where m is the number of scan cells in the circuit.

ž randomly choose two test vectors V_a and V_b from the actual test vector order f V_0; : : : ;

V_a; : : : ;V_b; : : : ;$V_{n\ 1}$g and exchange their position generating a new test vector order

f V_0; : : : ;V_b; : : : ;V_a; : : : ;$V_{n\ 1}$g, where n is the number of test vectors in the test set.

The alternative application of exchanges between randomly chosen test vectors and scan cells proves to be efficient in exploring the discrete design space. It should be noted that for partial scan sequential circuits the exchanges between test vectors are prohibited and *SA-Optimisation* from Figure 12 is not executing line 6. For each new solution the proposed best primary input change algorithm *BPIC-ALG*(S_{NEW} ;C_{NEW}) is called to determine the best primary input change times for all the test vectors from S_{NEW} according to the scan cell order in C_{NEW} . New solutions are either accepted or rejected depending on the acceptance criterion defined in the simulated annealing algorithm. If the best solution so far is reached then it is saved in f $S_{BE\ ST}$;$C_{BE\ ST}$ *g* which is returned together with best primary input change times at the end of the optimisation process. The optimisation process is terminated after the variation in the average cost over a selected number of sequences of solutions falls below a given value as described in. It should be noted that all the factors accountable for power dissipation during test application as described are included in the optimisation process.

ALGORITHM: SA-Optimisation
INPUT: Test Set S, Circuit C
OUTPUT: Best found test vector order f V_{B0} ; : : : ;$V_{Bm\ 1}$g
Best found scan cell orderfS_{B0} ; : : : ;$S_{Bm\ 1}$g
Best primary input change ft$_B$imes$_{01}$ n 1g
;t_B ; : : : ;t_B

1 Current test vector order is set to the initial test vector order
f$^V C_0$; : : : ;$^V C_{n\ 1}$ g f $^V I_0$; : : : ;$^V I_{n\ 1}$ g S_{INIT} *of S*
2 Current scan cell order is set to the initial scan cell order C_{INIT} *of C*
f$^S C_0$; : : : ;$^S C_{m\ 1}$ g f $^S I_0$; : : : ;$^S I_{m\ 1}$ g
3 repeat
4 repeat
5 Generate a new scan cell order C_{NEW} =*f* S_{N0} ; : : : ;$S_{Nm\ 1}$ g by swapping the positions of randomly chosen scan cells S_{Ci} *and* S_{Cj}
6 *Generate a new test vector order*S_{NEW} =*f*t_{N0} ; : : : ;$t_{Nn\ 1}$ g by swapping the positions of randomly chosen test vectors t_C *and* t_C
7 *compute NTC of the new solution and best primary input change times f*t_{N0} ; : : : ;$t_{Nn\ 1}$ g using *BPIC-ALG(S,C,f*S_{N0} ; : : : ;$S_{Nm\ 1}$ g)
8 if accepted according to the SA acceptance criterion [98] then
9 f$^S C_0$; : : : ;$^S C_m$ $_1$ g f $^S N_0$; : : : ;$^S N_m$ $_1$ g
10 if the best solution so far is reached then f
11 update S_{BEST} *and* C_{BEST} *with* S_{NEW} *and* C_{NEW}
12 f$^S B_0$; : : : ;$^S B_{m\ 1}$g f$^S N_0$; : : : ;$^S N_{m\ 1}$ g
13 f$^V B_0$; : : : ;$^V B_{m\ 1}$g f$^V N_0$; : : : ;$^V N_{m\ 1}$ g
14 f$^t B_0$; : : : ;$^t B_{n\ 1}$gfN_0 ; : : : ;$N_{n\ 1}$ g
15 g
16 until the number of solutions equals the solution sequence length
17 decrease the control parameter value according to the cooling schedule from
18 until the system is frozen

19 return f$^V B_0$; : : : ;$^V B_{m\ 1}$g f$^S B_0$; : : : ;$^S B_{m\ 1}$g f$^t B_0$; : : : ;$^t B_{n\ 1}$g

Figure 14: Proposed simulated annealing-based design space exploration for test vector and scan cell ordering and the proposed best primary input change (BPI application strategy

It is important to note that the size of the design space for partial scan sequential circuits is m!, and it is significantly smaller than the size of the design space for full scan sequential circuits m! n!, where m is the number of scan cells and n is the number of test vectors.[17] This is due to the fault activation and the fault-effect propagation sequences through non-scan cells which prohibit test vector ordering in the case of partial scan se-quintal circuits. While previous algorithms with no penalty in test area, performance, test efficiency, test application time or volume of test data, presented in use a *simple greedy heuristic* for asymmetric travelling salesman problem to find a *sub-optimal* test vector ordering for a given scan cell ordering, which is NP-hard, the proposed *BPIC-ALG* is an *exact* algorithm which always returns the *best (optimal)* primary input change times in *polynomial time* for a given scan cell ordering. However, when considering test vector and scan cell ordering the optimisation process for the discrete, degenerate and highly irregular design space makes the problem tractable only for small to medium sized scan sequential circuits.

Experimental Results

Experimental results are divided in three separate sections. It gives the results for a number of full scan sequential circuits. outlines the experimental results for partial scan sequential circuits, and Section highlights further benefits of partial scan in minimising power dissipation during test application.

Experimental Results for Full Scan Sequential Circuits

This section demonstrates through a set of benchmark examples that the proposed BPIC test application strategy yields savings in power dissipation during test application in full scan sequential circuits. Furthermore, the savings can be substantially improved when BPIC is integrated with test vector ordering and scan cell ordering as described in the algorithm. The *BPIC-ALG* and *SA-Optimisation* algorithms described. Were implemented within the framework of a low power testing system on a 350 MHz Pentium II PC with 64 MB RAM running Linux and using GNU CC.

The average value of node transition count (*NT C*) reported throughout this section, is calculated under the assumption of the zero delay model using Equation1. The use of zero delay models is motivated by very rapid computation of *NT C* required by the algorithms, and by the observation that power dissipation under the zero delay model has a high correlation with power dissipation under the real delay model. Besides, the aim of this chapter is not to give exact values of power dissipation during test application, but to *validate* the new BPIC test application strategy (Definition 5) for power minimisation that equally applies to every delay model. Further, although the power due to glitches is neglected in Equation 1, the zero delay model provides *reliable relative power information* that is reported throughout this experimental section. *Reliable relative power information* provided by *NT C* using the zero delay model means that savings in *NT C*, and savings in power dissipation obtained after technology mapping the circuit and accounting for glitching activity during test application, are within the same range. Therefore, to validate that experimental results using *NT C* reported throughout this section provide *reliable relative power information* appendix B shows that the savings in the case of the real delay model that accounts for glitching activity are even higher than the savings in the case of the zero delay model. This conclusion was reached after technology mapping circuit *s344* in AMS 0.35 micron technology [9], and using state of the art real delay model simulator with power and timing information. Furthermore, this result can also be explained by the fact that by eliminating spurious transitions (Definition 1) the propagation of hazards and glitches is also eliminated leading to even greater reductions in power dissipation in the case of the real delay model.

Table 3 shows the results when the BPIC test application strategy is applied by itself (i.e. without scan cell and test vector ordering) for 24 commonly accepted ISCAS89 benchmark circuits. The first and second columns give the circuit name and the number of scan cells (SC) respectively. The third column gives the number of test vectors (TV) generated by the ATPG tool ATOM. The average value of node transition count (*NT C*), which is the total value of *NT C* divided by the total number of clock cycles, for ASAP, ALAP, and the proposed BPIC test application strategies outlined, It can be clearly seen from Table 3 that BPIC test application strategy has the least average value of *NT C* for all the benchmark circuits when compared to ASAP and ALAP test application strategies. To give an indication of the reductions in average value of *NT C*, columns 7 and 8 show the percentage reduction of BPIC over ASAP and ALAP test application strategies. The reduction varies from approximately 10% as in the case of *s641* down to under 1% as in the case of *s526*. Table 3 has shown the reductions in node transition count using a non-compact test set. In order to reduce test application time while maintaining the same test quality, compact test sets are used. Compact test sets may lead to higher power dissipation because of an increased number of sensitised paths by each test vector. However, using the proposed BPIC test application strategy similar average values of *NT C* are achieved for all the benchmark circuits when comparing compact test sets to non-compact test sets. Table 4 shows experimental results for compact test set generated by MINTEST when applying the proposed BPIC test application strategy without scan cell and test vector ordering.[17] For example, in the case of *s298* the average value of *NT C* for non compact test set is 114.73 (Table3), whereas for compact test set the average value of *NT C* is 107.85 (Table 4) despite a considerable reduction in the number of test vectors from 52 as in the case of non-compact test set to 23 as in the case of the compact test set. The similar values of *NT C* are due to finding the best primary input change time for reducing spurious transitions during shifting in test vectors and shifting out responses. This clearly shows that using compact test sets and hence decreasing the test application time will *not* increase the power dissipation during test application in full scan sequential circuits.

circuit	SC	TV	ASAP NTC	ALAP NTC	proposed BPIC NTC	%reduction over ASAP	%reduction over ALAP	CPU time (s)
s208	8	65	55.39	55.73	53.48	**3.45**	**4.03**	0.17
s298	14	52	115.39	115.59	114.73	**0.56**	**0.74**	0.28
s344	15	62	131.43	131.45	130.54	**0.67**	**0.69**	0.48
s349	15	65	132.46	132.45	131.47	**0.75**	**0.74**	0.50
s382	21	72	145.12	145.54	143.91	**0.83**	**1.12**	0.80
s386	6	109	86.61	86.20	84.22	**2.76**	**2.29**	0.38
s400	21	71	146.32	146.35	144.78	**1.05**	**1.07**	0.81
s420	16	98	107.19	107.17	104.46	**2.53**	**2.52**	1.00
s444	21	77	149.08	149.93	148.05	**0.69**	**1.25**	0.97
s510	6	90	115.50	115.04	114.13	**1.17**	**0.79**	0.40
s526	21	107	185.83	186.17	184.79	**0.55**	**0.73**	1.45
s641	19	99	186.74	184.03	168.71	**9.65**	**8.32**	2.19
s713	19	100	198.88	196.83	180.42	**9.28**	**8.33**	2.29
s820	5	190	139.22	138.89	136.79	**1.74**	**1.51**	1.02
s832	5	200	138.46	137.96	136.05	**1.73**	**1.37**	1.07
s838	32	183	199.81	199.84	195.00	**2.40**	**2.42**	14.72
s953	29	138	169.93	169.66	167.20	**1.60**	**1.44**	4.71
s1196	18	227	105.18	105.35	100.43	**4.51**	**4.67**	6.38
s1238	18	240	106.85	107.43	102.06	**4.48**	**5.00**	6.69
s1423	74	135	508.09	509.91	502.78	**1.04**	**1.39**	56.48
s1488	6	196	346.62	346.92	342.76	**1.11**	**1.19**	2.68
s1494	6	191	351.92	352.85	348.54	**0.95**	**1.22**	2.62
s5378	179	358	1786.44	1786.58	1774.36	**0.67**	**0.68**	3113.87
s9234	211	660	3123.16	3123.33	3098.91	**0.77**	**0.78**	16395.37

Table 6: Experimental results for non-compact test set generated by ATOM when applying the proposed BPIC test application strategy without scan cell and test vector ordering

In the second experiment the test application strategy was changed to ALAP, and the results are shown in columns 4 and 5. In the third experiment the proposed BPIC test application strategy is combined with scan cell and test vector ordering and the results are given in columns 6 and 7. Note that BPIC always produces better results than ASAP and ALAP due to higher correlation between successive states during shifting in test vectors and shifting out test responses. This clearly shows the importance of integrating *all* the factors accountable for power dissipation in the optimisation process.[18] The reduction value depends on the type of the circuit and the average value of *NT C* for the initial scan cell and test vector order.

circuit	SC	TV	ASAP NTC	ALAP NTC	proposed BPIC NTC	%reduction over ASAP	%reduction over ALAP	CPU time (s)
s208	8	27	54.80	54.72	52.42	**4.35**	**4.20**	0.07
s298	14	23	108.25	108.57	107.85	**0.36**	**0.66**	0.12
s344	15	13	124.36	124.21	123.48	**0.70**	**0.58**	0.10
s349	15	13	128.35	128.33	127.62	**0.57**	**0.55**	0.10
s382	21	25	147.91	148.14	146.75	**0.78**	**0.93**	0.28
s386	6	63	85.77	85.26	83.38	**2.78**	**2.19**	0.21
s400	21	24	154.04	154.44	152.76	**0.83**	**1.08**	0.28
s420	16	43	100.73	100.46	98.12	**2.59**	**2.33**	0.48
s444	21	24	155.46	156.30	154.19	**0.81**	**1.35**	0.32
s510	6	54	114.03	113.75	112.53	**1.31**	**1.06**	0.24
s526	21	49	182.74	182.98	182.17	**0.31**	**0.44**	0.68
s641	19	21	172.88	176.55	161.08	**6.82**	**8.75**	0.47
s713	19	21	195.45	192.38	181.10	**7.34**	**5.86**	0.49
s820	5	93	138.03	137.65	135.55	**1.79**	**1.51**	0.51
s832	5	94	138.83	138.37	136.33	**1.79**	**1.47**	0.50
s838	32	75	187.95	187.56	185.14	**1.49**	**1.29**	6.35
s953	29	76	169.64	169.02	166.64	**1.76**	**1.40**	2.66
s1196	18	113	105.67	105.42	100.43	**4.95**	**4.73**	3.39
s1238	18	121	103.92	103.83	98.91	**4.82**	**4.74**	3.40
s1423	74	20	506.10	506.89	501.14	**0.98**	**1.13**	8.73
s1488	6	101	365.47	365.66	361.40	**1.11**	**1.16**	1.45
s1494	6	100	369.59	370.63	365.89	**1.00**	**1.28**	1.40
s5378	179	97	1808.88	1809.32	1791.68	**0.95**	**0.97**	826.89
s9234	211	105	3045.30	3045.51	3014.90	**0.99**	**1.01**	2637.05

Table 7: Experimental results for compact test set generated by MINTEST when applying the proposed BPIC test application strategy without scan cell and test vector ordering

For example in the case of *s713* the reduction is 34% and it goes down to 4% as in the case of *s838*. How-ever, this still presents an improvement when compared to ASAP and ALAP which yield reductions only of 3%. Table 6 shows the results for ASAP; ALAP and BPIC test application strategies when using compact test sets. Again the proposed BPIC provides better results than ASAP and ALAP, for all the circuits from the benchmark set. It is interesting to note that *NT C* values for the BPIC test application strategy when using non-compact and compact test sets are similar. This indicates that the test set size has no influence on

circuit	Test application strategy targeted during optimisation						CPU time (s)
	ASAP NTC	%reduction	ALAP NTC	%reduction	BPIC NTC	%reduction	
s208	48.39	12.64	49.19	11.19	**45.35**	**18.13**	24390
s298	97.97	15.09	92.49	19.84	**92.09**	**20.19**	33960
s344	115.55	12.08	119.68	8.93	**114.85**	**12.61**	34270
s349	118.62	10.45	121.01	8.64	**117.87**	**11.01**	35040
s382	125.93	13.22	125.98	13.18	**124.47**	**14.23**	40430
s386	70.50	18.60	71.86	17.03	**69.74**	**19.48**	41550
s400	128.97	11.85	132.12	9.70	**125.30**	**14.36**	34550
s420	93.94	12.35	94.51	11.82	**92.41**	**13.78**	43410
s444	130.27	12.61	134.33	9.89	**129.27**	**13.28**	42940
s510	98.91	14.35	101.60	12.02	**97.98**	**15.16**	36920
s526	162.13	12.75	160.96	13.37	**160.52**	**13.61**	37340
s641	142.19	23.85	141.44	24.25	**132.42**	**29.08**	42470
s713	146.91	26.13	144.98	27.09	**130.34**	**34.46**	44630
s820	111.71	19.75	112.10	19.47	**110.83**	**20.39**	43710
s832	115.19	16.80	114.07	17.61	**113.19**	**18.24**	36520
s838	193.50	3.16	193.80	3.01	**190.29**	**4.76**	45970
s953	128.24	24.53	128.61	24.31	**127.26**	**25.10**	46470

Table 8: Experimental results for non-compact test set generated by ATOM when applying the proposed BPIC test application strategy integrated with test vector ordering and scan cell ordering

the average value of *NT C* confirming that the only three accountable factors for power dissipation during test application in full scan circuits are test vector ordering, scan cell ordering and primary input change time. For some of the examples the computational time for completing the optimisation may increase over 40,000s using a Pentium II processor at 350 MHz, as shown in Table 7.[19] This is due to the huge size of the design space and the low number of solutions with identical *NT C* which clearly leads to longer times for exploration and convergence of the simulated annealing algorithm. However, when using compact tests as shown in Table 6, due to smaller number of test vectors and consequently the size design space, lower time for completion is required which leads to the conclusion that compact test sets have benefits in both test application time as well as in computational time with similar reductions in power dissipation.

circuit	Test application strategy targeted during optimisation						CPU time (s)
	ASAP NTC	%reduction	ALAP NTC	%reduction	BPIC NTC	%reduction	
s208	47.85	12.68	47.90	12.59	**44.02**	**19.67**	8399
s298	91.48	15.49	96.22	11.11	**91.13**	**15.81**	12980
s344	94.92	23.66	100.27	19.37	**94.02**	**24.39**	15550
s349	104.62	18.48	110.23	14.11	**104.14**	**18.85**	13560
s382	120.37	18.61	124.09	16.10	**118.49**	**19.88**	29020
s386	70.33	18.00	69.72	18.71	**68.54**	**20.09**	24500
s400	120.51	21.76	123.36	19.92	**119.51**	**22.41**	29380
s420	90.97	9.69	87.61	13.02	**83.13**	**17.47**	28940
s444	129.44	16.73	132.04	15.06	**120.07**	**22.76**	29040
s510	95.79	15.99	97.68	14.33	**94.80**	**16.86**	22940
s526	151.31	17.19	158.35	13.34	**150.87**	**17.44**	29310
s641	143.36	17.07	130.56	24.48	**120.16**	**30.49**	29210
s713	152.77	21.83	144.71	25.96	**133.49**	**31.69**	24920
s820	110.61	19.86	111.23	19.41	**109.71**	**20.51**	28870
s832	112.39	19.04	112.30	19.10	**111.40**	**19.75**	28950
s838	170.01	9.54	170.75	9.15	**168.36**	**10.42**	30220
s953	128.15	24.45	128.70	24.13	**127.06**	**25.09**	30040

Table 9 : Experimental results for compact test set generated by MINTEST when applying the proposed BPIC test application strategy integrated with test vector ordering and scan cell ordering

Experimental Results for Partial Scan Sequential Circuits
This section demonstrates through a set of benchmark examples that the proposed BPIC test application strategy outlined. Yields savings in power dissipation during test application in partial scan sequential circuits. Furthermore the savings can be substantially improved when the proposed BPIC test application strategy is combined with scan cell ordering.
Table 7 shows circuit and test set characteristic for 17 circuits from ISCAS89 bench-mark set. The first and second columns give the circuit name and the number of primary inputs respectively. The third and fourth columns give
the number of scan cells and non-scan cells respectively. The scan cells are selected using the logic level partial scan tool OPUS by cutting all the cycles in the circuit. Column 5 gives the number of test vectors generated by the logic level ATPG tool GATEST to achieve the fault coverage shown in the last column.

circuit	primary inputs	scan cells	non-scan cells	test vectors	fault coverage(%)
s344	9	5	10	41	99.41
s349	9	5	10	41	98.85
s382	3	9	12	112	98.74
s386	7	5	1	198	99.73
s400	3	9	12	128	97.40
s444	3	9	12	128	95.99
s510	19	5	1	70	100.00
s526	3	3	18	321	85.22
s641	35	7	12	104	94.64
s713	35	7	12	106	88.46
s820	18	4	1	283	99.88
s832	18	4	1	459	98.39
s953	16	5	24	206	100.00
s1423	17	22	52	257	95.31
s1488	8	5	1	221	100.00
s1494	8	5	1	232	99.20
s5378	35	30	149	1465	92.43

Table 10: Circuit and test set characteristic for 17 benchmark circuits from ISCAS89 benchmark set used in experimental results.

Table 8 shows the results when the proposed BPIC test application strategy is applied by itself (i.e. without scan cell ordering) for the 17 benchmark circuits described in Table 7. The average value of *NT C*, which is the total value of *NT C* divided by the total number of clock cycles over the entire test application period, for ALAP and the proposed BPIC test application strategies are given in columns 2 and 3 respectively. It can be clearly seen from Table 8 that BPIC test application strategy has smaller average value of *NT C* for all the benchmark circuits when compared to ALAP test application strategy. To give an indication of the reductions in average value of *NT C*, column 4 shows the percentage reduction of BPIC over ALAP test application strategy. The reduction value depends on the type of the circuit and the average value of *NT C* for the initial scan cell order. The reduction varies from approximately 15% as in the case of *s713* down to under 1% as in the case of *s349*. The last column gives the computational time for the exact *BPIC-ALG* algorithm, which computes best primary input change times used by BPIC test application time strategy. For most of the circuits it took approximately < 1s to find the best primary input change times for all the

circuit	initial ALAP *NT C*	proposed BPIC *NT C*	%reduction over initial ALAP	CPU time (s)
s344	85.39	84.14	**1.45**	0.10
s349	81.21	80.42	**0.98**	0.09
s382	78.92	77.48	**1.82**	0.44
s386	76.83	74.48	**3.06**	0.43
s400	81.22	79.87	**1.66**	0.52
s444	88.58	87.36	**1.36**	0.61
s510	104.13	102.54	**1.52**	0.23
s526	55.44	54.93	**0.91**	0.60
s641	98.55	85.47	**13.26**	0.80
s713	110.61	94.68	**14.40**	0.83
s820	120.26	117.78	**2.06**	1.01
s832	128.81	126.40	**1.87**	1.62
s953	95.85	93.00	**2.97**	1.16
s1423	186.82	183.60	**1.72**	10.78
s1488	318.00	311.72	**1.97**	2.14
s1494	326.87	321.91	**1.51**	2.23
s5378	523.49	498.88	**4.70**	380.11

Table 11: Reduction in average value of *NT C* when applying the proposed BPIC test application strategy compared to ALAP test application strategy

test vectors. This indicates that the proposed *BPIC-ALG* can be used for fast computation of the cost function in the optimisation process when combined with scan cell ordering as explained. There are exceptional circuits with very high number of test vectors (1465 in the case of *s5378*) where the computational time is up to 380s (last row from Table 8).

However, this is still acceptable low computational time for the calculation of the cost function. While the application of the proposed BPIC test application strategy reduces average value of *NT C* when compared to ALAP test application strategy, as shown in Table 8 further savings can be achieved when the proposed BPIC test application strategy is combined with scan cell ordering. Before combining scan cell ordering and the proposed the proposed BPIC test application strategy, the influence of scan cell ordering under the ALAP test application strategy [20] is examined as shown in Table 9. For circuits with small number of scan cells, the exploration of the entire design space is computationally inexpensive. In the case of *s713*, where for 7 scan cells there are 7! = 5040 possible scan cell orderings as outlined in Section, it took 3191s to find the optimum scan cell order which yields 11:42% reduction in average value of *NT C*.

circuit	initial ALAP *NT C*	Optimised ALAP *NT C*	%reduction over initial ALAP	CPU time (s)
s344	85.39	80.88	**5.28**	10
s349	81.21	79.77	**1.78**	10
s382	78.92	71.85	**8.95**	705
s386	76.83	70.81	**7.83**	45
s400	81.22	71.65	**11.78**	1258
s444	88.58	79.75	**9.96**	1618
s510	104.13	100.73	**3.62**	22
s526	55.44	55.30	**0.26**	3
s641	98.55	86.99	**11.72**	3039
s713	110.61	97.95	**11.42**	3191
s820	120.26	115.28	**4.14**	21
s832	128.81	120.34	**6.57**	33
s953	95.85	91.54	**4.49**	111
s1423	186.82	171.37	**8.26**	5989
s1488	318.00	305.49	**3.93**	214
s1494	326.87	310.46	**5.02**	224
s5378	523.49	394.88	**24.56**	44830

Table 12: Reduction in average value of *NT C* when applying scan cell ordering leading to optimised scan cell order under the ALAP test application strategy

However for larger circuits as in the case of *s1423* and *s5378* where the size of the design space is $22!t10^{21}$ and $30!t2{:}5\ 10^{32}$ respectively, *SA-Optimisation* algorithm is required for efficient design space exploration of the discrete, degenerate and highly irregular design space. For example it takes up to 44830s to

find an sub-optimum scan cell order as in the case of *s5378*. This is due to the huge size of the design space and the low number of solutions with identical *NT C* which clearly leads to long computational times for the convergence of the simulated annealing algorithm. It should be noted that for most of the benchmark circuits scan cell ordering under ALAP test application strategy (Table 9) yields higher reductions in average value of *NT C* than when the proposed BPIC test application strategy is applied by itself (Table10), at the expense of significantly greater computational time. Furthermore, there are circuits (*s641* and *s713*) where the proposed BPIC test application strategy applied by itself generates higher reductions in *NT C* with computational time which is three orders of magnitude lower when compared to scan cell ordering under the ALAP test application strategy.

circuit	initial ALAP *NT C*	Optimised BPIC *NT C*	**%reduction over initial ALAP**	CPU time (s)
s344	85.39	79.93	**6.39**	57
s349	81.21	79.18	**2.50**	57
s382	78.92	71.17	**9.81**	4895
s386	76.83	68.65	**10.64**	265
s400	81.22	70.66	**13.01**	3117
s444	88.58	78.98	**10.83**	5570
s510	104.13	99.57	**4.37**	127
s526	55.44	54.80	**1.15**	12
s641	98.55	76.99	**21.87**	25390
s713	110.61	85.58	**22.62**	25170
s820	120.26	113.19	**5.87**	100
s832	128.81	118.37	**8.10**	162
s953	95.85	89.49	**6.63**	683
s1423	186.82	169.61	**9.21**	26270
s1488	318.00	299.81	**5.71**	1257
s1494	326.87	306.02	**6.37**	1321
s5378	523.49	373.26	**28.69**	121700

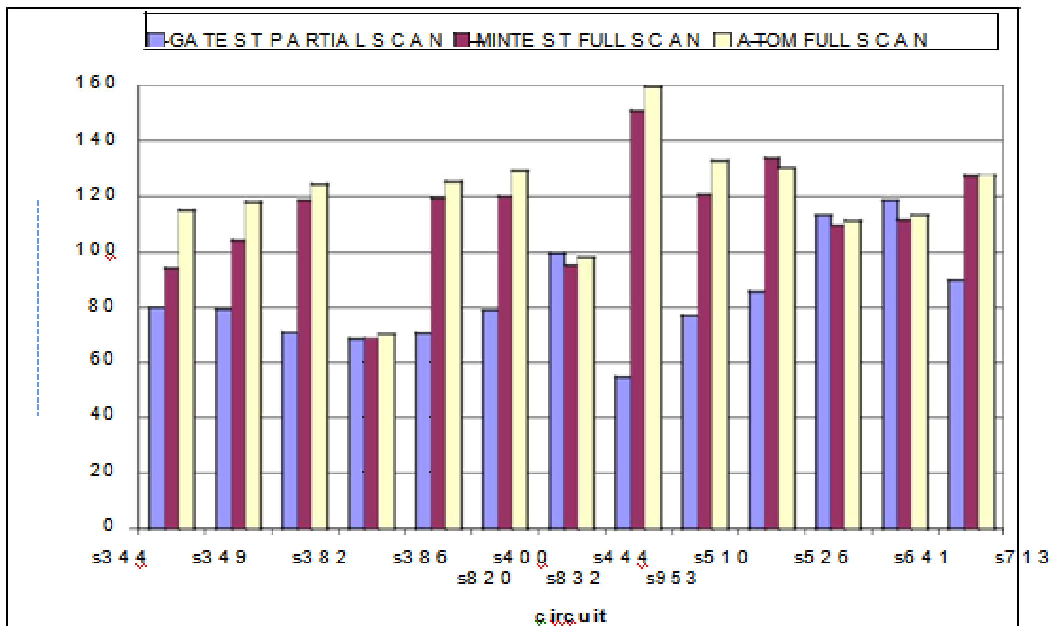
Table 13: Reduction in average value of *NT C* when combining the proposed BPIC test application strategy with scan cell ordering leading to optimised scan cell order under the BPIC test application strategy

For example, in the case of *s713* it took 3191s to achieve 11:42% reduction in average value of *NT C* by scan cell ordering (last two columns of Table12) when compared to only 0:80s of computational time to achieve 14:40% reduction in average value of *NT C* by the proposed BPIC test application strategy (last two columns of Table 8). To achieve maximum reductions in average value of *NT C*, the proposed BPIC test application strategy and scan cell ordering are combined as shown in Table 13. For all the benchmark circuits the combination of the BPIC test application strategy and scan cell ordering leads to higher reductions than when any parameter is considered by itself. For example in the case of *s5378* the reduction in average value of *NT C* is 28.69% at the expense of high computational time which is due to high number of scan cells and hence large design space and low convergence of the simulated annealing algorithm.

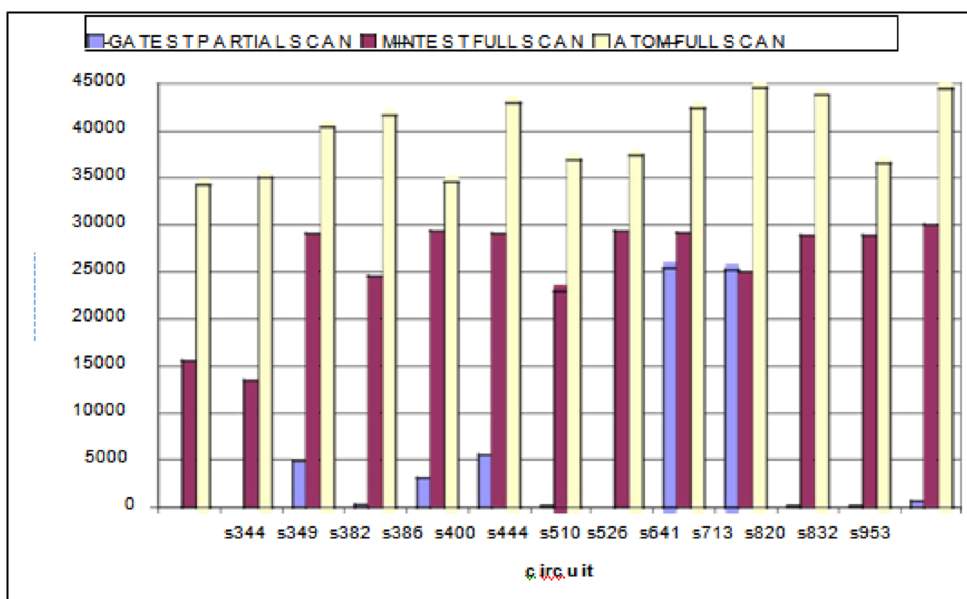
Further Benefits of Partial Scan in Minimising Power Dissipation in Scan Based Sequential Circuits

It is known that partial scan has advantages in terms of test area overhead and test application time when compared to full scan [3]. This section shows how the proposed BPIC test application strategy for partial scan provides further benefits in terms of power dissipation and computational time required for design space exploration when compared to full scan. Figures 13(a) and 13(b) show a comparison of average value of *NT C* and computational time for partial and full scan sequential circuits for various benchmark circuits. The results for full scan sequential circuits were outlined in Table 5 (ATOM), and Table 6 (MINTEST). The average value of *NT C* for partial scan is significantly smaller when compared to full scan, as shown in Figure 13(a). The reduction is due to partial scan DFT methodology, which in the test mode of operation does not clock the non-scan cells while test responses are shifted out, leading to significant savings in power dissipation. It is interesting to note that for benchmark circuits *s820* and *s832* the average value of *NT C* is lower for full scan sequential circuits. This is due to the fact that for both circuits 4 out of 5 sequential elements are modified to scan cells and

full scan sequential circuits allow test vector ordering which gives higher degree of freedom during the optimisation process. However, the processing time is significantly lower for partial scan sequential circuits as shown in Figure 13(b) which gives a comparison of computational overhead. It should be noted that large circuits (*s1423* and *s5378*) are not handled in the case of the full scan sequential circuits due to the huge size of the design space where both scan cell and test vector ordering are considered. Furthermore,
for all the benchmark circuits shown in Figure 13(b) the computational time required for exploring the design space of partial scan is substantially smaller (orders of magnitude) than the computational time required for exploring the design space of full scan. This is caused by the reduction in the size of the design space to be explored due to smaller number of scan cells and by the exact and polynomial time *BPIC-ALG* algorithm. Finally, based on the results shown in Figures 13(a) and 13(b), it may be concluded that partial scan has advantages not only in less test area overhead and test application time, but also in less power dissipation during test application (i.e. average value of *NT C* in Figure 13(a)) and computational time required for design space exploration (CPU time in Figure 13(b)) when compared to full scan.



(a) Average value of *NT C*



(b) Computational time

Figure 14: Comparison of average value of NT C and computational time for partial and full scan sequential circuits when using the proposed BPIC test application strategy

Concluding Remarks

This chapter has proposed a new technique for minimising power dissipation in full scan sequential circuits during test application. The technique is based on increasing the correlation between successive states during shifting in test vectors and shifting out test responses by changing the primary inputs such that the smallest number of transitions is achieved. A new algorithm, which is test set dependent, computes best primary input change (BPIC) time for each test vector was presented. It was shown that combining the described technique with scan cell and test vector ordering, using a simulated annealing-based design space exploration, reductions in power dissipation during test application in small to medium sized full scan sequential circuits are achieved. Exhaustive experimental results using both compact and non-compact test sets have shown that compact test sets have similar power dissipation during test application with reduction in test application time and computational time when compared to non-compact test sets.

The new BPIC test application strategy introduced in Definition 3 is equally applicable to minimising power dissipation in partial scan sequential circuits. Since test vector ordering proposed for power reduction in full scan sequential circuits is prohibited for partial scan sequential circuits, the proposed test application strategy yields power reduction as shown in the experimental results. Since the proposed test application strategy depends only on controlling primary input change time, power is minimised with no penalty in test area, performance, test efficiency, test application time or volume of test data. It was shown that combining the proposed BPIC test application strategy and scan cell ordering using a simulated annealing-based design space exploration algorithm yields reductions in power dissipation during test application in partial scan sequential circuits.

This chapter has shown that partial scan does not provide only the commonly known benefits such as less test area overhead and test application time, but also less power dissipation during test application and computational time required for design space exploration, when compared to full scan. This reinforces that partial scan should be the preferred choice as design for test methodology for sequential circuits when low power dissipation during test application is of prime importance for high yield and reliability.

References:

[1]. S.T. Chakradhar and S. Dey. Resynthesis and retiming for optimum partial scan. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 18(5):621–630, May 1999.

[2]. S. Chakravarty, J. Monzel, V.D. Agrawal, R. Aitken, J. Braden, J. Figueras, S. Ku-mar, H.J. Wunderlich, and Y. Zorian. Power dissipation during testing: Should we worry about it? In *15th IEEE VLSI Test Symposium (VTS)*, page 456, 1997.

[3]. P.R. Chalsani, S. Bhawmik, A. Acharya, and P. Palchaudhuri. Design of testable VLSI circuits with minimum area overhead. *IEEE Transactions on Computers*, 38(9):1460–1462, September 1989.

[4]. A.P. Chandrakasan and R.W. Brodersen. *Low Power Digital CMOS Design*. Kluwer Academic Publishers, 1995.

[5]. A.P. Chandrakasan, M. Potkonjak, R. Mehra, J. Rabaey, and R.W. Brodersen. Optimizing power using transformations. *IEEE Transactions on Computer-Aided De-sign of Integrated Circuits and Systems*, 14(1):12–31, January 1995.

[6]. S.-C. Chang, K.-J. Lee, Z.-Z. Wu, and W.-B. Jone. Reducing test application time by scan flip-flops sharing. *IEE Proceedings - Computers and Digital Techniques*, 147(1):42–48, January 2000.

[7]. C.-S. Chen and T.T. Hwang. Layout driven selection and chaining of partial scan flip flops. *Journal of Electronic Testing: Theory and Applications (JETTA)*, 13(1):19–27, August 1998.

[8]. C.I.H. Chen. Graph partitioning for concurrent test scheduling in VLSI circuits. In *Proc. 28th Design Automation Conference (DAC)*, pages 287–290, 1991.

[9]. K.-T. Cheng. Gate level test generation for sequential circuits. *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 1(4):405–442, October 1996.

[10]. K.-T. Cheng and A. Krstic. Current directions in automatic test-pattern generation. *Computer*, 32(11):58–64, November 1999.

[11]. V. Chickername, J. Lee, and J.K. Patel. Addressing design for testability at the architectural level. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 13(7):920–934, July 1994.

[12]. V. Chickername and J.H. Patel. An optimization based approach to the partial scan design problem. In *Proc. International Test Conference*, pages 377–386, 1990.

[13]. V. Chickername and J.H. Patel. A fault oriented partial scan design approach. In *Proc. International Conference on Computer Aided Design*, pages 400–403, 1991.

[14]. D.G. Chimney and K. Keutzer. Closing the gap between ASIC and custom: An ASIC perspective. In *Proc. 37th IEEE/ACM Design Automation Conference (DAC)*, pages 637–642, 2000.

[15]. S. Chiu and C.A. Papachristou. A design for testability scheme with applications to data path synthesis. In *Proc. 28th IEEE/ACM Design Automation Conference (DAC)*, pages 271–277, 1991.

[16]. R.M. Chou, K.K. Saluja, and V.D. Agrawal. Scheduling tests for VLSI systems under power constraints. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 5(2):175–184, June 1997.

[17]. S.-H. Chow, Y.-C. Ho, T. Hwang, and C.L. Liu. Low power realization of finite state machines - a decomposition approach. *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 1(3):313–340, July 1996.

[18]. F. Corno, P. Prinetto, M. Rebaudengo, and M. Sonza-Reorda. A test pattern generation methodology for low power consumption. In *16th IEEE VLSI Test Symposium*, pages 453–460, 1998.

[19]. F. Corno, M. Rebaudengo, M. Sonza Reorda, G. Squillero, and M. Violante. Low power BIST via non-linear hybrid cellular automata. In *18th IEEE VLSI Test Sym-posium*, pages 29–34, 2000.
[20]. F. Corno, M. Rebaudengo, M. Sonza Reorda, and M. Violante. A new BIST architecture for low power circuits. In *IEEE European Test Workshop (ETW99)*, pages 160–164, 1999.

International Journal of Engineering Science Invention (IJESI) is UGC approved Journal with Sl. No. 3822, Journal no. 43302.

Prof.Dr.G.Manoj Someswar "Power Minimisation in Scan Sequential Circuits Based On Best Primary Input Change Time" International Journal of Engineering Science Invention (IJESI), vol. 07, no. 02, 2018, pp. 10–38.