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Retiming Of Fixed Point Digital Filter for Critical Path Reduction

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Abstract: *This Work Describes A Circuit Transformation Technique Called Retiming In Which Registers And Added At Some Points In A Circuit And Removed From Others In Such A Way That The Functional Behavior Of The Circuit As A Whole Is Preserved. We Show That Retiming Can Be Used To Transform A Given Synchronous Circuit Into A More Efficient Circuit Under A Variety Of Different Cost Criteria. We Model A Circuit As A Graph In Which The Vertex Set V Is A Collection Of Combinational Logic Elements And The Edge Set E Is The Set Of Interconnections Each Of Which May Pass Through Zero Or More Registers. We Employ Retiming To A Fixed Point Digital Filter To Reduce The Critical Path Delay.*

Keywords – *Retiming, Fir Filter,Forward Retiming. Backward Retiming, Feed Forward Cutest Retiming*

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I. Introduction

Retiming Is The Technique Of Moving The Structural Location Of Latches Or Registers In A Digital Circuit To Improve Its Performance, Area, And/Or Power Characteristics In Such A Way That Preserves Its Functional Behavior At Its Outputs. The Technique Uses A Directed Graph Where The Vertices Represent Asynchronous Combinational Blocks And The Directed Edges Represent A Series Of Registers Or Latches (The Number Of Registers Or Latches Can Be Zero). Each Vertex Has A Value Corresponding To The Delay Through The Combinational Circuit It Represents. After Doing This, One Can Attempt To Optimize The Circuit By Pushing Registers From Output To Input And Vice Versa - Much Like Bubble Pushing. Two Operations Can Be Used - Deleting A Register From Each Input Of A Vertex While Adding A Register To All Outputs, And Conversely Adding A Register To Each Input Of Vertex And Deleting A Register From All Outputs. In All Cases, If The Rules Are Followed, The Circuit Will Have The Same Functional Behavior As It Did Before Retiming.

Retiming Is A Powerful Design Optimization Technique. However, Retiming Algorithms Have A Large Cost That Limits Their Use: The Efficient Retiming Of Large Circuits Remains Computationally Very Demanding, Even Though Sophisticated Optimization Techniques Have Been Introduced. Register Retiming Is A Circuit Optimization Technique That Moves Registers Forward Or Backward Across Combinational Elements In A Circuit. The Aim Of This Procedure Is To Shorten The Clock Cycle Or Reduce Circuit Area.

Retiming Is A Technique For Optimizing Sequential Circuits. It Is A Procedure That Repositions The Registers In A Circuit Leaving The Combinational Portion Unchanged.

The Main Objective Of One Form Of Retiming Is To Find A Circuit With The Minimum Number Of Registers For A Specified Clock Period.

1. To Reduce The Critical Path Using Retiming Of The Digital Circuit.
2. To Changing The Position Of Existing Delay Elements.
3. To Improve Circuit Performance By Optimizing Combinational Delay.

II. Methodology

Block Diagram

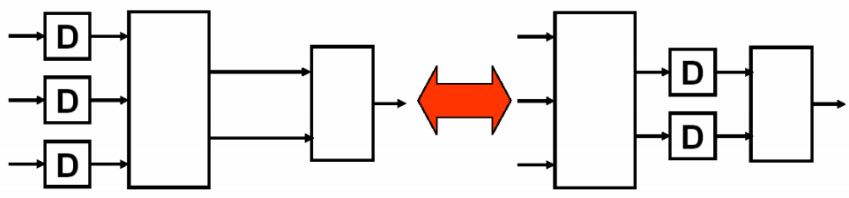

Fig 2.1 (A) Block Diagram For Retiming

Retiming Means Changing The Position Of Existing Delay Elements. Retiming Improves Circuit Performance By Optimizing Combinational Delay. Difference Between Retiming And Pipelining Is Retiming Does Not Change The Input/Output Behavior Of The System.

Basics Of Register Retiming: There Are Two Basic Types Of Register Retiming: Forward Retiming And Backward Retiming. Forward Retiming Refers To Removing A Fixed Number Of Registers From Each Input Or A Gate And Inserting The Same Number Of Registers At The Output. Conversely, In Backward Retiming We Remove A Fixed Number Of Registers From The Output Of A Gate And Insert The Same Number Of Registers In Front Of Each Input. Let Us First Consider An Example Of Forward Retiming In A Circuit With Simple Edge- Triggered Flip-Flops. In The First Part Each Input Of The Or Gate Is Driven By A Q- Pin Of A Register. Furthermore, Both Of These Registers Have Identical Clock Signals. Therefore, It Is Possible To Remove One Register From Each Input Of The Or Gate And Instead Insert One Register On The Output. Notice That The Two Registers In The Original Version Became One Register In The Retimed Version; Therefore, The New Circuit Has A Smaller Area. Even More Importantly, If We Re-Synthesize The Logic Of The Retimed Circuit, It Is Possible To Eliminate The First Two Gates, Thereby Making The Circuit Even Smaller.

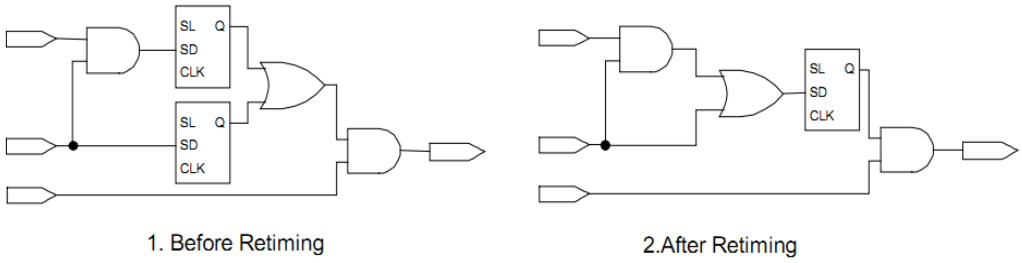

Fig 2.2(A) Forward Retiming.

Conversely, In Backward Retiming, A Register Is Deleted From All The Direct Fanouts Of A Gate And A New Register Is Inserted In Front Of Every Input Of The Gate. Figure 3.2 Illustrates This Concept And Also Shows How Retiming Can Be Used To Shorten The Clock Cycle. Notice That Before Retiming, The Critical Path Of The Circuit In Went Through Three Gates, Whereas After Retiming, This Path Has Been Shortened To Two Gates. This Allows Us To Increase The Clock Speed.

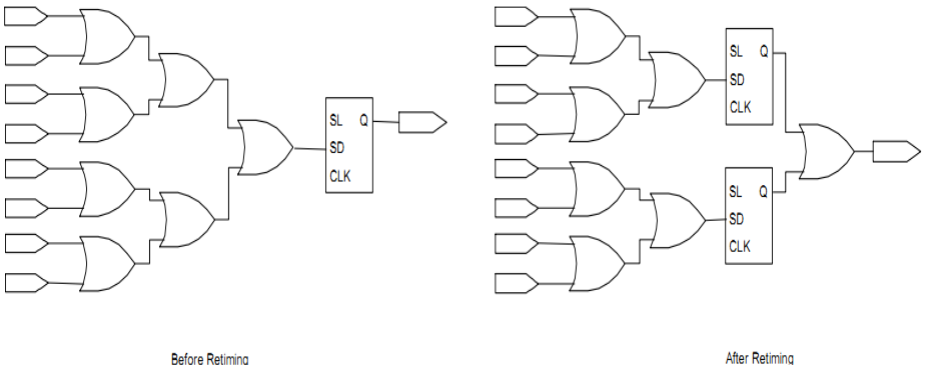

Fig 2.2(B) Backward Retiming

III. Data Flow Graphs

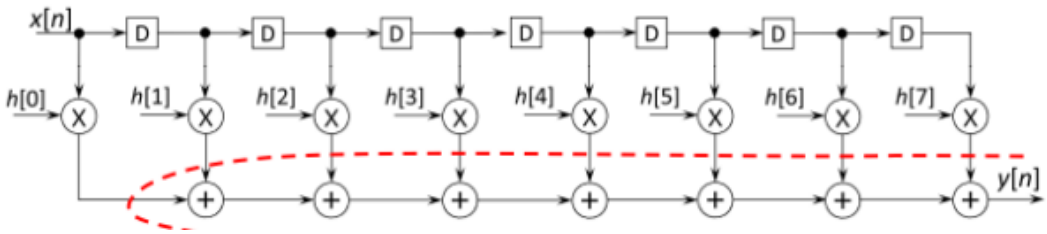

Fig 3.1 (A) Dfg Of Fir Filter Of Length N = 8.

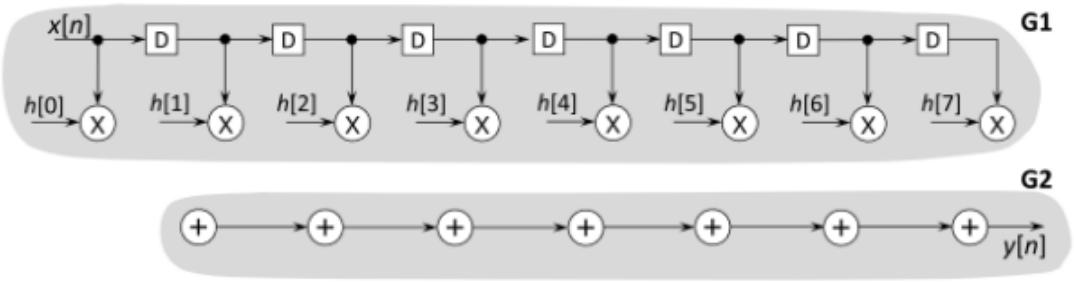

Fig 3.1 (B) Decomposition Of Dfg To Two Subgraphs G1 And G2 For Feed-Forward Cutset Retiming Of Dfg.

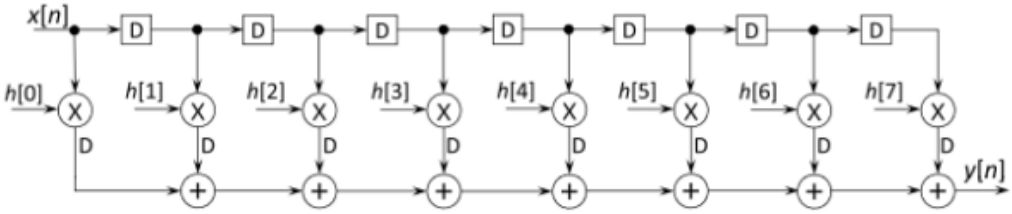

Fig. 3.2(A) Retimed Dfg.

Flexible Retiming Of Fir Filter Based On Connected Component Timing Model: We Discuss Here A Flexible Scheme For The Retiming Of The Dfg Of Fig. 3.1(A). To Perform The Desired Retiming The Direction Of Accumulation Path In The Dfg Is Reversed [As Shown In Fig. 3.1(A)], And The Cutsets Across The Dashed Lines (After Each Gray Box) Are Considered One After The Other For Retiming.

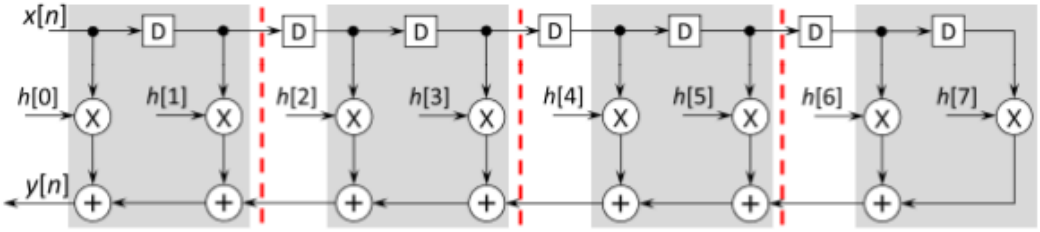

Fig.3.3(A) Cutset Selection For The Proposed Retiming Of Dfg Of The Fir Filter Of Length N = 8.

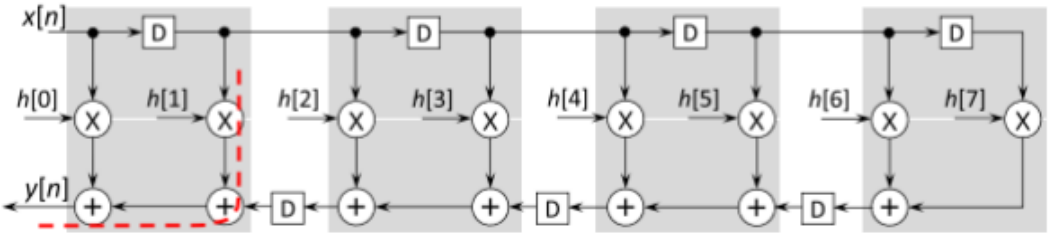

Fig.3.3(B) Retimed Dfg.

IV. Conclusion

The Proposed Techniques Can Be Helpful For Less Pipeline Overheads As Exact Estimation Of Propagation Delays Can Be Made By Connected Component Model, Which Results Easy Way To Obtain Exact Estimation Of Propagation Delays Over Different Paths In Dfg. The Advantage Of Proposed Retiming Technique Is Critical Path Reduction, Later It Shown That The Splitting And Merging Of Nodes May Results Less Combination Path Delays. This Techniques Of Fixed Point Circuits Can Be Extended To Floating Point Circuits. These Methods Could Be Useful In Digital Signal Processing And Fir, Iir Filters.

V. Future Scope

Currently, The Cost Model Only Considers The Hardware Cost Of Arithmetic Components, Other Components, E.G. Memories, Interfaces, Were Assumed Occupying Insignificant Resources. A More Accurate Model Can Be Developed, Which Will Take These Factors Into Account. Moreover, Timing Constraint Can Also Be Considered, E.G. Logic Delay, Clock Cycles Can Be Added Into The Cost. A More Robust Error

Reporting Mechanism Can Be Used. For Example, Each Object Can Be Associated With A Flag, Which Can Indicate Arithmetic Error, Such As Overflow And Underflow, Occurred During Simulation.

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