International Journal of Engineering Science Invention (IJESI)
ISSN (Online): 2319 – 6734, ISSN (Print): 2319 – 6726
www.ijesi.org ||Volume 7 Issue 9 Ver I || Sep 2018 || PP 17-29

Power Quality Improvement and Fault Current Interruption by the Dynamic Voltage Restorer Based On Fuzzy Logic Controller

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Abstract-- *In this paper we introduce and evaluate a control strategy for downstream fault current interruption in a radial distribution line by means of a dynamic voltage restorer (DVR). The proposed Fuzzy Logic Controller supplements the voltage-sag compensation control of the DVR. It does not require phase-locked loop and independently controls the magnitude and phase angle of the injected voltage for each phase. Fast least error squares digital filters are used to estimate the magnitude and phase of the measured voltages and effectively reduce the impacts of noise, harmonics, and disturbances on the estimated phasor parameters and this enables effective fault current interrupting even under arcing fault conditions. The results of the simulation studies performed in the MATLAB/SIMULINK platform indicate that the proposed control scheme: 1) can limit the fault current to less than the nominal load current and restore the point of common of coupling voltage within 10ms: 2) can interrupt the fault current in less than two cycles: 3) limits the dc-link voltage rise, and thus, has no restrictions on the duration of fault current interruption: 4) performs satisfactorily even under arcing fault conditions: 5) can interrupt the faultcurrentunderlowdc-linkvoltageconditions.*

Index Terms— Digital filters, Dynamic Voltage Restorer (DVR), fault current interruption, multiloopcontrol,Fuzzylogiccontroller(FLC).

Date of Submission: 31-08-2018 Date of acceptance: 15-09-2018

I. Introduction

The contemporary container craneindustry like many other industry segments is often enamored by the bells and whistles, colorful diagnostic displays, high speed performance, and levels of automation that can be achieved. Although these features and their indirectly related computer based enhancements are key issues to an efficient terminal operation, we must not forget the foundation upon which we are building. Power quality is the mortar which bonds the foundation blocks.Powerqualityalsoaffectsterminaloperating economics, crane reliability, our environment, and initial investment in power distribution systems to support new crane installations. To quote the utility company newsletter which accompanied the last monthly issue of my home utility billing: Using electricity wisely is a good environmentaland

Business practice which saves you money, reduces emissions from generating plants, and conserves our natural resources. As we are all aware, container crane performance requirements continue to increase at an astounding rate. Next generation container cranes, already in the bidding process, will require average power demands of 1500 to 2000kW– Almost double the total average demand three years ago. The rapid increase in power demand levels, an increase in container crane population, SCR converter crane drive retrofits and the large AC and DC drives needed to power and control these cranes will increase awareness of the power quality issue in the very near future. The American "sag" and the British "dip" are both names for a decrease in voltage to between 10 and 90% of nominal voltage for one-half cycle to one minute sagsaccount for the vast majority of power problems experienced by end users. They can be generated both internally and externally from an end users facility. External causes of sags primarily come from the utility transmission and distribution network. Sags coming from the utility have a variety of cause including lightning, animal, human activity, normal and abnormal utility equipment operation. Sags generated on the transmission or distribution system can travel hundreds of miles thereby affecting thousands of customers during a single event. Sometimes externally caused sags can be generatedbyothercustomersnearby.

The starting of large electrical loads or switching off shunt capacitor banks can generate sag large enough to affect a local area. If the end userisalreadysubjecttochronicundervoltage,then even relatively small amplitude sag can have detrimental effects. Sags caused internally to an end users facility are typically generated by the starting of large electrical loads such as motors or magnets. The large inrush of current required to starts these types of loads depresses the voltage level available to other equipment that share the same electrical system. As with externally caused sags, ones generated internally will be magnified by chronic under voltage. The dynamic voltage restorer (DVR) is a facts device utilized to counteract voltage sags [1], [2]. It injects

controlled three-phase ac voltages in series with the supply voltage, subsequent to a

Voltagesag, to enhance voltage quality by adjusting the voltage magnitude, wave shape, and phase angle [3]–[6]. Fig. 1 shows the main components of a DVR (i.e,a series transformer T_S, a voltage- source converter (VSC), a harmonic filter, a dc-side capacitor $C_{D¢}$, and an energy storage device [7], [8]). The line side harmonicfilter

[5]Consistsoftheleakageinductanceoftheseries transformer$L_f$and the filtercapacitorC_f.

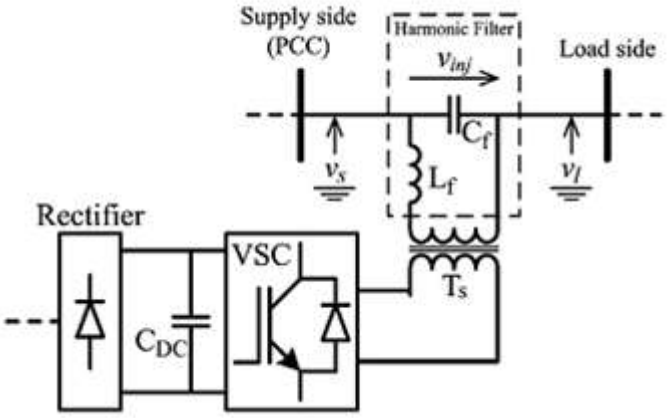

Fig.1. SchematicdiagramofaDVRwithaline-side harmonicfilter.

The DVR conventionally bypassed during a downstream fault to prevent potential adverse impacts on the fault and to protect the DVR components against the fault current [9]–[11]. A technically elaborate approach to more efficient utilization of the DVR is to equip it with additional controls and enable it also to limit or interrupt the downstream fault currents. A control approach to enable a DVR to serve as a fault current limiter is providedin[9].The maindrawbackofthisapproach is that the dc-link voltage of the DVR increases due to real power absorption during fault current- limiting operation and necessitates a switch to bypass the DVR when the protective relays, depending on the fault conditions, do not rapidly clear the fault. The dc-link voltage increase can be mitigated at the cost of as low-decaying dc fault current component using the methods introduced in [7] and[12].

To overcome the aforementioned limitations, this paper proposes an augmented control strategy for the DVR that provides: 1) voltage-sag compensation under balanced and unbalanced conditions and 2) a fault current interruption (FCI) function. The former function has been presented in [13] and the latter is described in thispaper.

It should be noted that limiting the fault current by the DVR disables the main and the backup protection (e.g., the distance and the over current relays). This can result in prolonging the fault duration. Thus, the DVR is preferred to reduce the fault current to zero and interrupt it and send a Trip signal to the upstream relay or the circuit breaker(CB).

It should be noted that the FCI function requires 100%voltage injection capability. Thus, the power ratings of the series transformer and the VSC would be about three times those of a conventional DVR with about 30%–40% voltage injection capability. This leads to a more expensive DVR system. Economic feasibility of such a DVR system depends on the importance of the sensitive load protected by the DVR and the cost of the DVR itself.

The performance of the proposed control scheme is evaluated through various simulation studies in the MATLAB/SIMULINK platform. The study results indicate that the proposed control strategy: 1) limits the fault current to less than the nominal load current and restores the PCC voltage within less than 10 ms, and interrupts the fault current within two cycles; 2) it can be used in four- and three- wired distribution systems, and single-phase configurations; 3) does not require phase-locked loops; 4) is not sensitive to noise, harmonics, and disturbances and provides effective fault current interruption even under arcing fault conditions; and 5) can interrupt the downstream fault current under low dc-link voltageconditions.

Proposed fcicontrol strategy

The adopted DVR converter is comprised of three independent H-bridge VSCs that are connected to a common dc-link capacitor. These VSCs are series connected to the supply grid, each through a single- phase transformer. The proposed FCI control system consists of three independent and identical controllers oneforeachsingle-phaseVSCoftheDVR.

Assume the fundamental frequency components of the supply voltage v_S, load voltage v_l , and the injected

voltage v_{inj}, Fig. 1are

$$v_S = V_S \times \cos(wt+\Theta_S) \quad (1)$$

$$v_l = V_l \times \cos(wt+\Theta_l) \quad (2)$$

$$v_{inj} = v_S - v_l = V_{inj} \times \cos(wt+\Theta_{inj}) \quad (3)$$

Two identical least error squares (LES) filters [14] are used to estimate the magnitudes and phase angles of the phasors corresponding to and (i.e., $\bar{V}_S = V_S \angle \Theta_S$ and $\bar{V}_{inj} = V_{inj} \angle \Theta_{inj}$, respectively in 5ms [13]).

The FCI function requires a phasor parameter estimator (digital filter) which attenuates the harmonic contents of the measured signal. To attenuate all harmonics, the filter must have a full-cycle data window length which leads to one cycle delay in the DVR response. Thus, a compromise between the voltage injection speed and disturbance attenuation is made. This filter also performs satisfactorily in the FCI operation mode, even under arcing fault conditions where the measured voltage and current signals are highlydistorted.

Fig. 2 shows a per-phase block diagram of the proposed DVR control system corresponding to the FCI operation mode, where is the nominal rms phase voltage. The control system of Fig. 2 utilizes v_S, v_l, the dc-link voltage V_{DC}, and the harmonic filter capacitor current i_{cap} as the input signals. The reported studies in this paper are based on the over current fault detection method of [7] and [12]. The fault detection mechanism for each phase is activated when the absolute value of the instantaneous current exceeds twice the rated loadcurrent.

The proposed multi loop control system [3], [8], [9], [15]–[20] includes an outer control loop (voltage phasor control) and an inner control loop (instantaneous voltage control). The inner loop provides damping for the transients caused by the DVR harmonic filter [18] and [21], and improves the dynamic response and stability of the DVR. The inner loop is shared by the sag compensation and the FCI functions. When a downstream fault is detected, the outer loop controls the injected voltage magnitude and phase angle of the faulty phase(s)and reduces the load-side voltage to zero, to interrupt the fault current and restore the PCC voltage. The DVR "outer" voltage phasor control and "inner" instantaneous voltage control, corresponding to each phase, are describedinthefollowingtwosubsections.

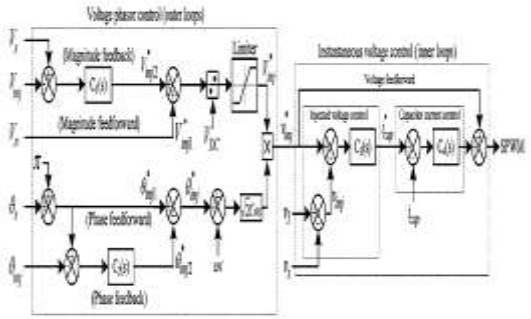

Fig.2. Per-phase block diagram of the DVR control system in FCImode.

Controls the injected voltage magnitude and phase angle of the faulty phase(s) and reduces the load-side voltage to zero, to interrupt the fault current and restore the PCC voltage. The DVR "outer" voltage phasor control and "inner" instantaneous voltage control, corresponding to each phase, are described in the following twosubsections.

A. Voltage Phasor Controlsystem

In the FCI operation mode, the required injected voltage phasor is equal to the source voltage phasor, but in phase opposition [i.e. the injected phasor, $\bar{V}_S = V_{inj} \angle \Theta_{inj}$ is controlled to be $V_S \angle (\Theta_S + \Pi)$]. Performance of the voltage phasor control, in terms of

transient response, speed, and steady-state error, is enhancedbyindependentcontrolofvoltagemagnitude and phase, and incorporating feed forward signals to the feedback control system [17], [18], [21]–[27]. Fig. 2 shows two fuzzy logic controllers (C1 and C2) that are used to eliminate the steady-state errors of the magnitude and phase of the injected voltage, respectively. Parameters of each controller are determined to achieve a fast response with zero steady-state error. Control of the proposed DVR is basedonfuzzylogicbasedfeedbackcontroller.

Fuzzy Logic controller

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC. The FLC comprises of three parts: Fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular

membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the heightmethod.

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM(PositiveMedium),andPB(PositiveBig).The

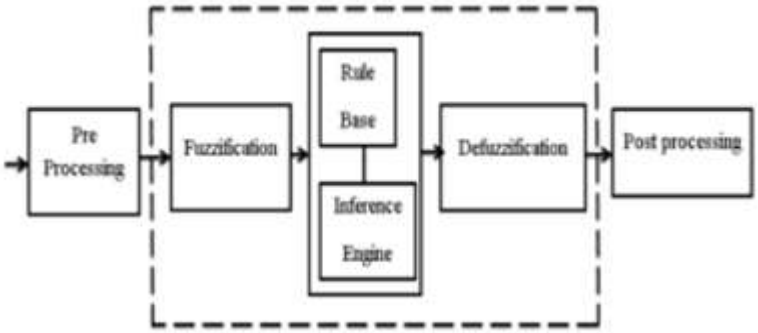

Fig.3. Fuzzy logiccontroller

Partition of fuzzy subsets and the shape of membership*CE(k) E(k)* function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor

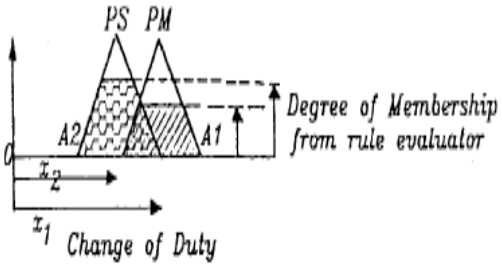

Fig.4. Defuzzificationusingcenterofgravity method.

Table I FuzzyRules

Change inerror	Error						
	NB	NM	NS	Z	PS	PM	PB
NB	PB	PB	PB	PM	PM	PS	Z
NM	PB	PB	PM	PM	PS	Z	Z
NS	PB	PM	PS	PS	Z	NM	NB
Z	PB	PM	PS	Z	NS	NM	NB
PS	PM	PS	Z	NS	NM	NB	NB
PM	PS	Z	NS	NM	NM	NB	NB
PB	Z	NS	NM	NM	NB	NB	NB

In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular *E(k)* input there is only one dominant fuzzy subset. The input error for the FLC is givenas

$\underline{P_{ph(k)}-P_{ph(k-1)}}$

needed. To compute the output of the FLC, „height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error andoutput

The set of FC rules are derivedfrom
u=-[αE +(1-α)*C]
Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable. A large value of error E indicates that given system is not in the balanced state. If the system is unbalanced, the controller should enlarge its control variables to balance the system as early as possible. One the other hand, small value of the error E indicatesthatthesystemisneartobalancedstate.

B. InstantaneousVoltageControlsystem

Under ideal conditions, a voltage sag can be effectively compensated if the output of the phasor- based controllerv^* is directly fed to thesinusoidal
Pulse-width modulation (SPWM) unit. However, resonances of the harmonic filter^{inj} cannot be eliminated under such conditions. Therefore, to improve the stability and dynamic response of the DVR, an instantaneous injected voltage controller and a harmonic filter capacitor current controller are used to

$$E(k)= V_{ph(k)} - V_{ph(k-1)}$$

ttenuateresonances.
The generated reference signalfor theinjected
*
CE(k) = E(k) –E(k-1)

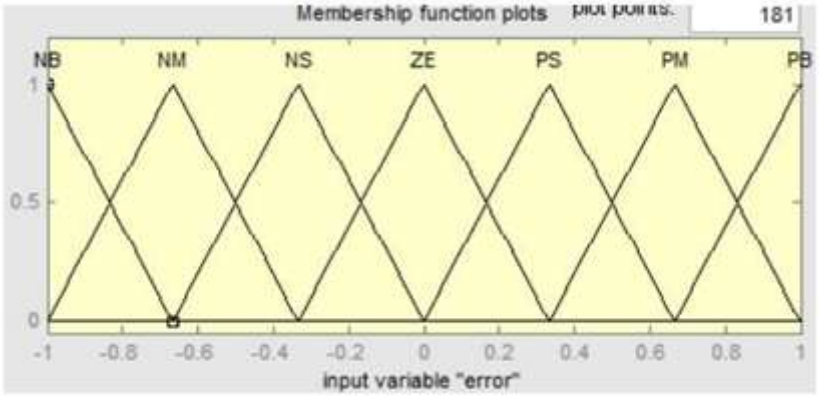

Fig.5. Membershipfunctions

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by theminimumoperatorandmaximumoperator.Table1 shows rule base of theFLC.

Defuzzification: As a plant usually requires a non- fuzzy value of control, a defuzzification stage is voltage v_{inj} is compared with the measured injected voltage$_{cap}$, and the error is fed to the voltage controller. As shown in Fig. 2, the output of the voltagecontroller i^* is the reference signal for the filter capacitor currentcontrol loop. It is compared with the measured capacitor current i_{cap} , and the error is fed to the currentcontroller.
The steady-state error of the proposed control system is fully eliminated by the FLC controllers in the outer control loop (i.e. C_1 and C_2), whichtrackdcsignals(magnitudeandphaseangle).

II. Studyresults

Fig.6 depicts a single-line diagram of a power system which is used to evaluate the performance of the proposed DVR control system under different fault scenarios, in the MATLAB/SIMULINK software environment. A 525-kVA DVR system is installed on the 0.4-kV feeder, to protect a 500-kVA, 0.90 lagging power factor load against voltage sags. Parameters of the simulated power system and the DVR are given in
Appendix A. In the reported studies, the base voltage for per-unit values is the nominal phase voltage. Besides, voltage and current waveforms of phases A, B, and C are plotted by solid, dashes, and dotted lines, respectively.

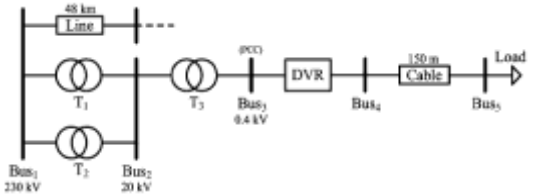

Fig.6. Single-line diagram of the system used for simulationstudies

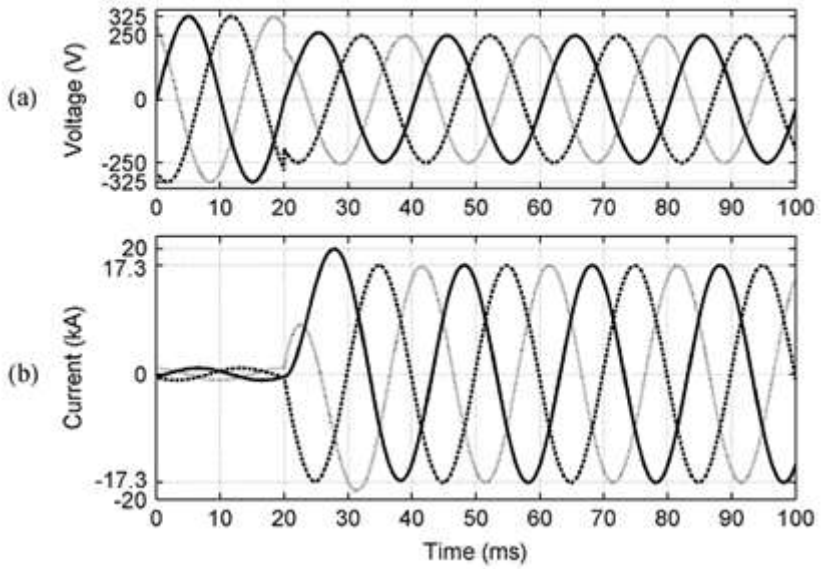

Fig.7.(a) Voltages at bus3 (b) Fault currents, during downstream three-phase fault when the DVR is inactive(bypassed).

A. Three-PhaseDownstreamFault

Thesystemissubjectedtoathree-phaseshort circuit with a negligible fault resistance at t=20 ms at Bus5 . Prior to the fault inception, the DVR is inactive (in standby mode) (i.e., the primary windings of the series transformers are shorted by the DVR). During the fault if the DVR is bypassed, the voltage at Bus3 drops to 0.77 p.u. and the fault current increases to about 17 times the rated load current (Fig. 8). Fig. 8 shows FCI performance of the proposed DVR control system during the fault. Fig. 7(a)–(c), respectively, shows the three-phase injected voltages, the restored three-phase supply-side voltages, and the three-phase load-side voltages which are reduced to zero to interrupt the fault currents. The slightly injected voltage by the DVR beforetheaultinitiation[Fig8(a)]isthevoltagedropacrosstheseriesimpedanceof theDVRseriestransformersecondarywinding.

Fig. 8(d) shows the line currents (i.e., the currents passing through the DVR). Fig. 8(d) illustrates that the proposed FCI method limits the maximum fault current to about 2.5 times the nominal value of the load current and interrupts the fault currents in less than 2 cycles. Fig. 8(e) depicts variations of the dc- link voltage during the FCI operation, and indicates that the dc-link voltage rise under the worst case (i.e., a severe three phase fault) is about 15% and occurs duringthefirst5msafterfaultinception.

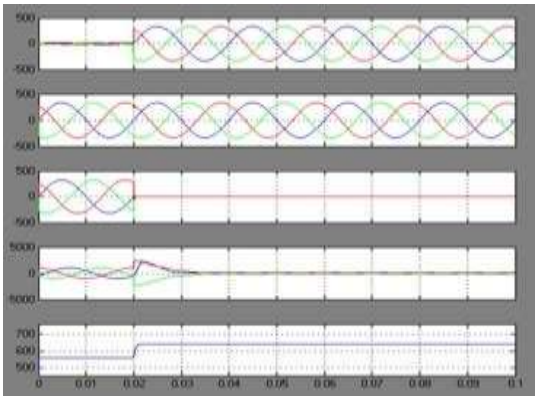

Fig.8.(a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, duringthethree-phasedownstreamfault.

A. Phase–to-Phasedownstreamfault

The system of Fig.6 is subjected to a phase-A to phase-C fault with the resistance of 0.05 at 10% of the cable length connecting Bus4 to Bus5,at 20 rms. When the DVR is inactive (bypassed) during the fault (Fig.9), the PCC voltage drops to 0.88 p.u., and the fault current increases to about 11 times the rated loadcurrent.

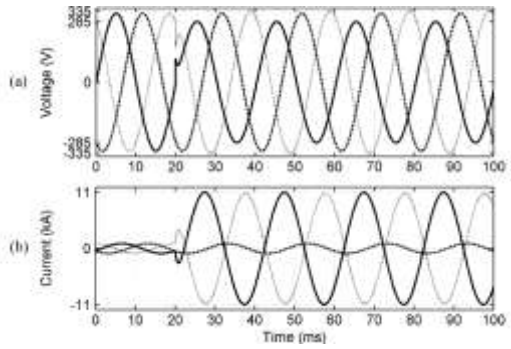

Fig.9.(a) Voltages at bus3 , (b) Fault currents, during downstream phase-to-phase downstream faultwhentheDVRisinactive(bypassed).

Fig.10 illustrates that when the DVR is in service,the proposed FCI control successfully interrupts the fault current and restores the PCC voltage of the faulty phases within two cycles. Fig. 10(e) shows that the dc-link voltage rise is less than 7%. Fig.9 also shows that only the two faulty phases of the DVR react, and thehealthyphaseisnotinterrupted.

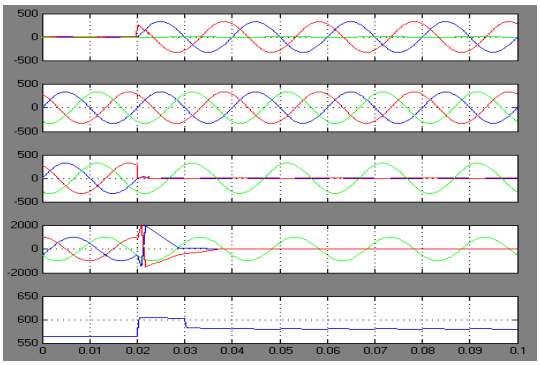

Fig.10.(a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, duringthephase-to-phasedownstreamfault.

B. Singlephasetogrounddownstreamfault

Phase-A of the system of Fig. 6 is subjected to a fault with the resistance of 0.2 at 10% length of the cable connecting Bus4 to Bus5 , at 20ms. If the DVR is inactive (Fig.11),the PCC voltage does not considerably

drop and the fault current is about 2.5

p.u. It must be noted that although the PCC voltage drop is not considerable, the fault current must be interrupted by the DVR to prevent possible damages to the VSC before the fault is interrupted by the relays. The reason is that the operation time of the over current relays is Considerable for a fault current of about2.5p.u.Fig.12illustratesthattheproposedDVR control strategy successfully interrupts the fault current in the faulty phase in about two cycles. Fig. 11(e) shows that the dc-link voltage rises less than 1.8%. Fig. 13 also shows that only the faulty phase of the DVR reacts to fault current, and the healthyphases are notinterrupted.

Simulation studies conclude that the dc-link voltage rise caused by the proposed FCI mode of operation is proportional to the fault current, and depends on the type of fault. The results also indicate that the maximum dc-link voltage rise occurs under the most severe three-phase fault which is about 15%, and can betoleratedbasedonDVRappropriatedesign.

It must be noted that to prevent operation of three- phase induction motors under unbalanced voltage conditions, they must be equipped with protective devices which detect such conditions and disconnect the load when any of the phases is de-energized by the single-phase operation of the FCI function. Furthermore, disabling the single-phase fault current interruption capability can be provided as an operational option and the operator can decide either touseordisablethisfunctiondependingonthetypeof load.

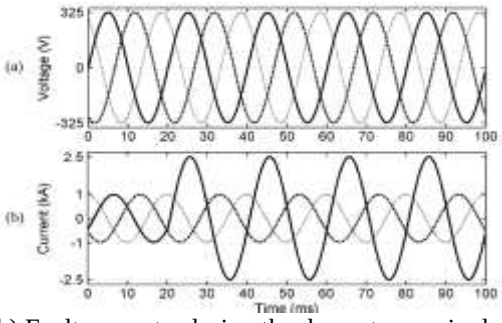

Fig.11. (a) Voltages at Bus3 (b) Fault currents, during the downstream singlephase-to-ground fault when the DVR is inactive(bypassed).

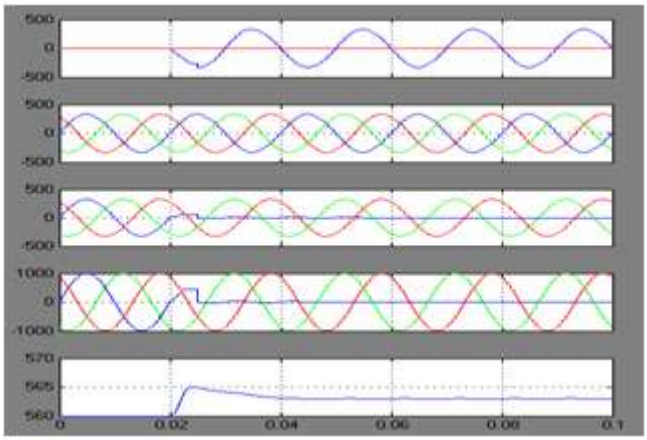

Fig.12.(a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, duringthesingle-phase-to-grounddownstreamfault.

C. Effect of the Fault v-iCharacteristic

Due to the nonlinear v-i characteristic of a free- burning arc, the voltage and current waveforms are highly distorted during an arcing fault. To investigate the effects of such distortions on the performance of the proposed FCI control scheme, a single phase-to- ground downstream arcing fault at Bus5 is considered. The arc is modeled based on the modified Cassie– Mayr equations [28]. The effect of variation of the arc length on the arc voltage [29] is also taken into account.

The fault is initiated at 15 ms on phase A. When the DVR is inactive (bypassed), Fig.13 ,the PCC voltage drops to 0.87 p.u., and the fault current rises to about

9.5 p.u. Fig.13 shows the time-varying nonlinear - characteristic of the arc during this fault. Fig. 13 shows the PCC voltage, and the fault current waveforms are highly distorted as a result of the fault V-I characteristic. This is confirmed by the frequency spectrum of the voltage waveform as depicted in Fig. 15.

The performance of the proposed FCI control scheme during the arcing fault is illustrated in Fig.16. Itshows

that the proposed control strategy successfully interrupts the arcing fault current in the faulty phase in half a cycle (i.e., even faster than that of the bolted fault conditions). The reason is that the resistance of the arcing fault provides higher damping for the decayingdccomponentofthefaultcurrent.

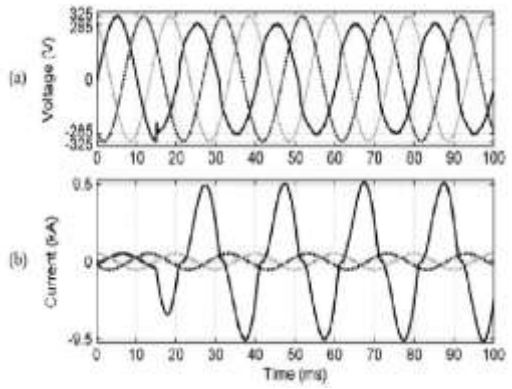

Fig.13. (a) Voltages at Bus3 (b) Fault currents, during the downstream single phase-to-ground arcing fault whentheDVRisinactive(bypassed).

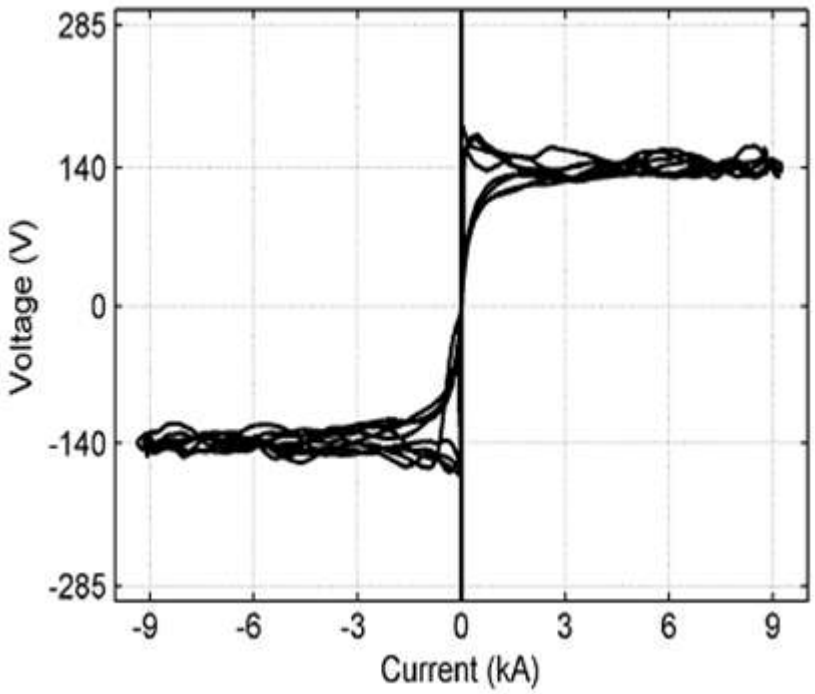

Fig. 14. Nonlinear v-i characteristic of thearc.

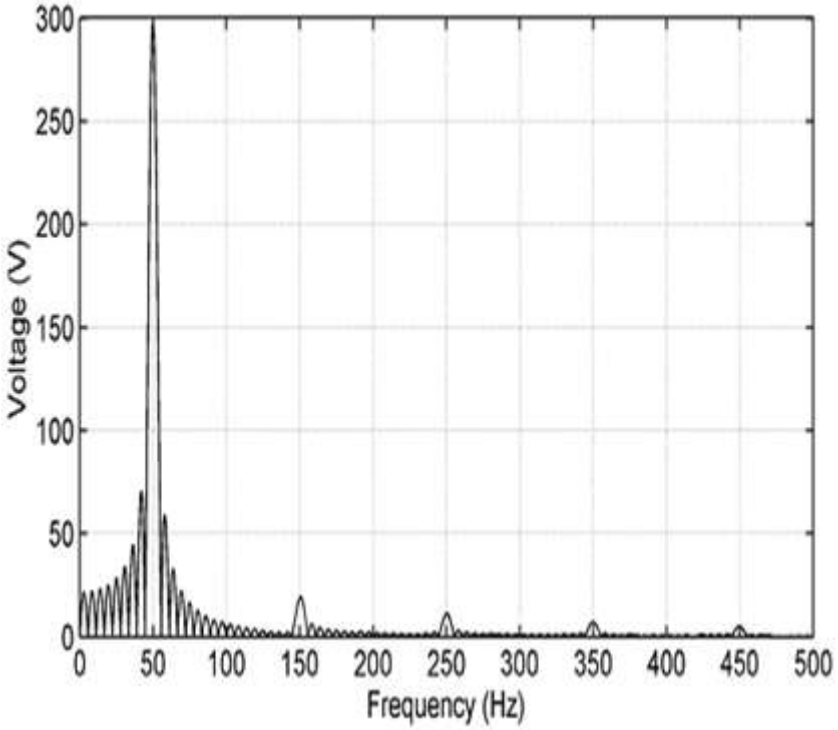

Fig.15. Harmonic content of voltage at during the arcingfault

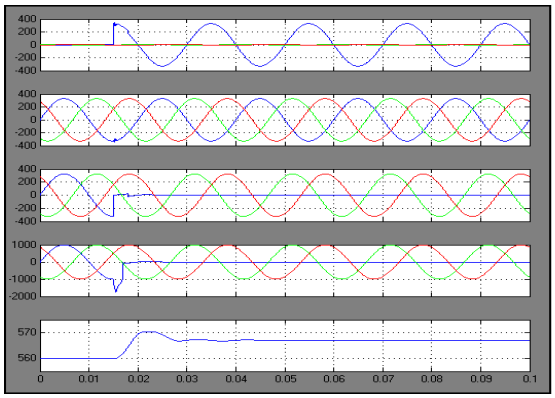

Fig.16.(a)Injectedvoltages.(b)Sourcevoltages.(c) Load voltages. (d) Line currents. (e) DC-link voltage, during the single-phase-to-ground downstream arcingfault.

E. SimultaneousFCIOperationandSag Compensation

The proposed DVR control system performs two different functions (i.e., sag compensation and FCI). Thus, the mutual effects of these modes on each other must be evaluated. At t=15 ms, the system of Fig. 6 is subjected to a phase-A to phase-B fault with the resistance of 1Ω at 90% of the line length from Bus1. The fault causes 87% voltage sag at the PCC. At

55 ms, another fault with the resistance of 0.2 on phase-A at 10% length of the cable connecting Bus4 to Bus5 occurs. The upstream fault is cleared by relays att

= 93ms.

Fig. 17 shows the performance of the proposed DVR control system under the aforementioned conditions (i.e., simultaneous FCI operation and sag compensation). Fig. 17 shows that when the downstream fault occurs in phase-A, the operation mode of the DVR in phase-A changes from sag compensation to FCI operation. However, the DVR continues to compensate the sag in phase-B to restore the load voltage in this phase. Consequently, phase-A and phase-B of the DVR operate in sag compensation mode during 15< t < 55 ms. During 55<t<93 ms, phase-A is in FCI operation mode, and phase-B continues to compensate the sag. During t > 93 ms, phase-B is in standby mode since the upstream fault is cleared and phase-A continues to interrupt the downstream fault current. During the entire process, phase-C is in standbymode.

Fig. 17(d) depicts variations of the dc-link voltage and Indicates that the dc-link voltage drops during

sag compensation, but the FCI operation maintains the dc- link voltage when it is lower than a certain value (the dc-link voltage, which is needed to reduce the load voltage to zero). This continues until the capacitor voltage approaches the aforementioned threshold. The reason is that when the capacitor voltage is lower than a certain value, the magnitude of the voltage injected

by the DVR, which must be 180º out of phase with respect to the source voltage, is less than the source voltage magnitude. Thus, small current flows through the DVR until the capacitor is charged. This current results in active power absorption by theDVR.

Fig. 18 shows the effect of lower initial dc-link voltage on the FCI operation during a phase-A to ground fault with the Mresistance of 0.05 Ω at 10% length of the cable connecting Bus4 to Bus5, at 15 ms. If the DVR is inactive (bypassed) during the fault, the fault current increases to about 7 times the rated load current. Fig. 18(a) shows that even under very low dc- link voltage conditions, the FCI control limits the fault current to less than the nominal load current in about one cycle. Fig.18(b)shows that regardless of the initial dc-linkvoltage, thedc-linkcapacitorischargeduptoa voltage which is adequate to inject a voltage equal to thesupplyvoltageandfullyinterruptthefaultcurrent.

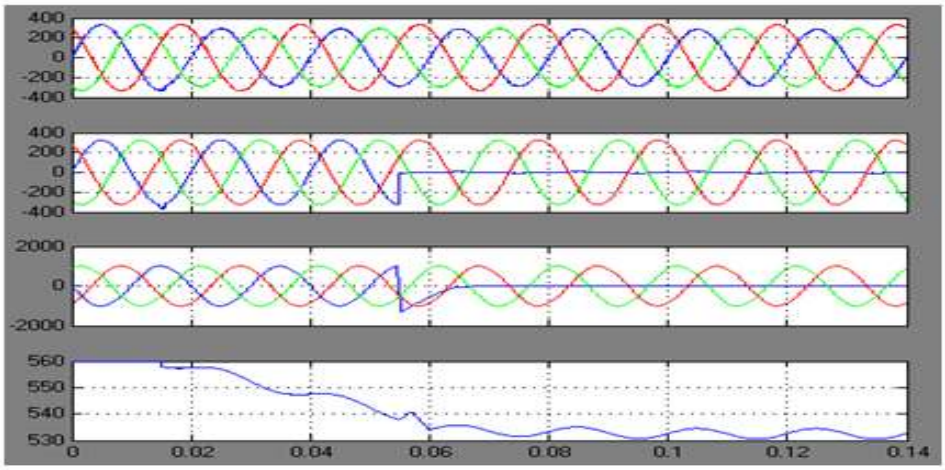

Fig.17.(a) Source voltages. (b) Load voltages. (c) Line currents. (d) DC-link voltage, during phase-A to ground downstream fault which takes place during sag compensation in phases A andB.

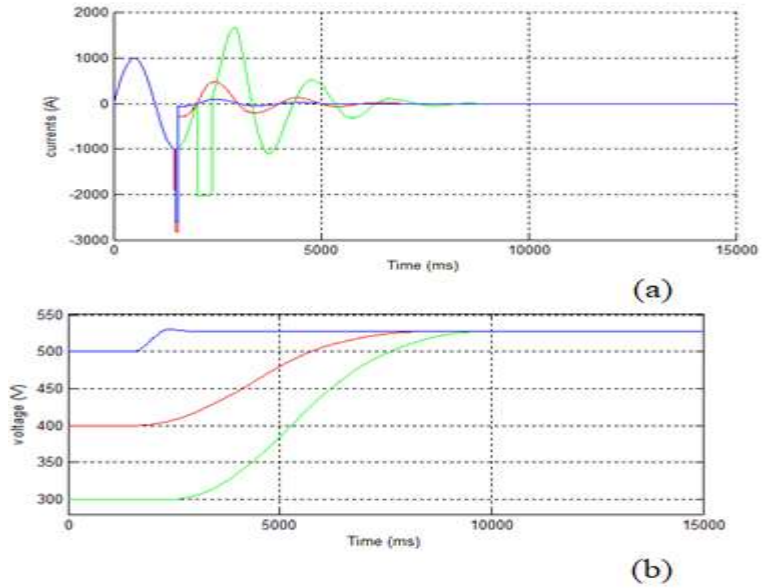

Fig.18.(a) Line current of phase-A and (b) dc-link voltage, for different initial values of the dc-link voltage,duringdownstreamphase-A-to-groundfault.

III. Conclusion

This paper introduces an improved control mechanism to enable the DVR to interrupt downstream fault currents in a radial distribution feeder with the help of fuzzy logic controller. This control function is an addition tothevoltage-sagcompensationcontroloftheDVR.Theperformanceof theproposedcontroller,underdifferentfaultscenarios, including arcing fault conditions, is investigated based on time-domain simulation studies in the MATLAB/SIMULINKenvironment.Thestudyresults concludethat:

- The proposed multi loop control system provides a desirable transient response and steady-state performance and effectively damps the potential resonant oscillations caused by the DVR LC harmonicfilter;
- Theproposedcontrolsystemdetectsandeffectively interrupts the various downstream fault currents within twocycles;
- The proposed fault current interruption strategy limits the DVR dc-link voltage rise, caused by active power absorption, to less than 15% and enables the DVR to restore the PCC voltage without interruption; in addition, it interrupts the downstream fault currents even under low dc-link voltageconditions.
- The proposed control system also performs satisfactorily under downstream arcing fault conditions.

APPENDIXA

DVR MODELPARAMETERS

Parameters of the studied power system and the DVR areasfollows.ShortcircuitcurrentatBUS1:31.5KV, X/R at Bus_1: 5.67; w=2*π*50rad/s

Transmission line (48km)

R_{Line} = 1.876 Ω, L_{Line} = 0.0774H

TABLE I TRANSFORMER PARAMETERS

Cable (150km)

Transformer	T_1T_2	T_3	T_s
Rated	90	2	0.1
No load	0.00	0.002	0.0
Copperlosses	0.004	0.009	0.0
Leakagereactance (p.u)	0.23 7	0.06	0.0 5
Primaryvoltage rating(KV)	230	20	0.4
Secondaryvolta ge	20	0.4	0.2 45
Winding connection	YnD	DYn	---

TABLEII

VSCPARAMETERS

Parameter	**Value**
Switchingfrequency(unipolarSPWM)	3kHZ
DC-link ratedvoltage	560V
DC- linkcapacitor	100mf
Harmonic filter capacitorC_f	300μ_f
Harmonic filter inductor L_f(leakage inductance ofT_s)	56.82 μH

R_{cable} = 9.6 mΩ, L_{cable} = 340mH

Parameters of the step-down transformers T1 ,T2 , and T3, and the DVR series transformers are given in Table I. Parameters of the VSC are given in TableII

In FCI operation mode, each single-phase series transformer should be able to inject 1-p.u. line-to- neutral voltage (231 V).Taking into account the voltage drop across its series branch impedance under the nominal load current of 721 A and the safety margin needed to prevent over modulation during transients, the secondary

voltage rating of the series transformer is chosen to be 245 V. Therefore, the power rating of $T_s$is 245 x 721= 175 kVA, and the ratingoftheDVR is3x175=525kVA.

References

[1]. N. G. Hingorani, "Introducing custom power,"IEEE Spectr., vol. 32, no. 6, pp. 41–48, Jun.1995.

[2]. J. G. Nielsen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump," in Proc. IEEE APEC', 2001, pp.1267–12

[3]. G. J. Li, X. P. Zhang, S. S. Choi, T. T. Lie, and Y. Z. Sun, "Control strategy for dynamic voltage restorers to achieve minimum power injection without introducing sudden phase shift," Inst. Eng. Technol. Gen.Transm.Distrib.,vol.1,no.5,pp.847–853,2007.

[4]. S. S. Choi, B. H. Li, and D. M. Vilathgamuwa, "Design and analysis of the inverter-side filter used in the dynamic voltage restorer," IEEE Trans. Power Del., vol. 17, no. 3, pp. 857–864, Jul. 2002. 91 0 IEEE TRANSACTIONS ON POWER DELIVERY, VOL. 28, NO. 2, APRIL2013

[5]. B. H. Li, S. S. Choi, and D. M. Vilathgamuwa, "Design considerations on the line-side filter used in the dynamic voltage restorer," P ro c . I n s t . E l e ct. E n g . , G e n . Tr a n s m . D i s t r i b ., vol. 148, no. 1, pp. 1–7, Jan.2001.

[6]. S. S. Choi, B. H. Li, and D. M. Vilathgamuwa, "Dynamic voltage restoration with minimum energy injection," I E E E Tr a n s . P o we r . S y st, vol. 15, no. 1, pp. 51–57, Feb. 2000.

[7]. Y. W. Li, D. M. Vilathgamuwa, P. C. Loh, and F. Blaabjerg, "A dualfunctional medium voltage level DVR to limit downstream fault currents," I E E E Tr a n s . P o w e r . E l e c t ro n ., vol. 22, no. 4, pp. 1330– 1340, Jul.2007.

[8]. Y. W. Li, D. M. Vilathgamuwa, F. Blaabjerg, andP.C. Loh, "A Robust control scheme for medium- voltage-level DVR implementation," I E E E Tr a n s . I n d . E l e c t ro n . , vol.54,no.4,pp.2249– 2261,Aug.2007.

[9]. S. S. Choi, T. X. Wang, and D. M. Vilathgamuwa, "A series compensator with fault current limiting function," I E E E Tra n s . P o w e r D e l . , vol. 20, no. 3, pp. 2248–2256, Jul.2005

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Dr. M. Sandeep " Power Quality Improvement and Fault Current Interruption by the Dynamic Voltage Restorer Based On Fuzzy Logic Controller:" 'International Journal of Engineering Science Invention(IJESI), vol. 7, no. 9, 2018, pp. 17-29