International Journal of Engineering Science Invention (IJESI)
ISSN (Online): 2319-6734, ISSN (Print): 2319-6726
www.ijesi.org ||Volume 9 Issue 3 Series.II || Mar.2020 || PP 09-16

Desigin of OfdmTransmitter and Reciever with Programmable Fft

G.S.N. Murthy[1], B. Venkatesh[2], Ch. Hemalakshmi[3],Dr.ShaikMastan Vali[4]
[1]*B. Tech Student Department of ECE, MVGR College of Engineering, Vizianagaram.*
[2]*B. Tech Student Department of ECE, MVGR College of Engineering, Vizianagaram.*
[3]*M.Tech Student Department of ECE, MVGR College of Engineering, Vizianagaram.*
[4]*Professor, Department of ECE, MVGR College of Engineering, Vizianagaram.*

Abstract:*System–on-a-chip (SoC) is now a trend in digital design because it gives a lot of advantages over discrete electronic based product such as higher speed, lower power consumption, smaller size, lower cost etc. In this project single chip Orthogonal Frequency Division Multiplexing (OFDM) transmitter and receiver have been designed using Verilog. OFDM is a multi carrier modulation technique used in the various digital communication systems like 3G GSM, WiMAX and 4Getc. The main advantage of this transmission technique is its robustness to channel fading in wireless communication environment. There are many applications of OFDM in communication such as digital audio broadcasting, Asynchronous Digital Subscriber Line (ADSL) and High bit-rate Digital Subscriber Line (HDSL) systems. In OFDM, two algorithms digital signal processing algorithm Fast Fourier transform (FFT) and Inverse Fast Fourier Transform (IFFT) are mainly involved. The 8-point IFFT/FFT Decimation-InFrequency (DIF) with radix-2 algorithm has been analyzed and incorporated in the design. The design has been simulated on the FPGA platform with Nexys 4 DDR KIT simulator. Simulation results show that each of the modules of the proposed OFDM is working as desired. The test output achieved from the simulation result of the OFDM has been verified with that of the Model Sim output.*

Keywords:—*OFDM (Orthogonal Frequency Division Multiplexing), FFT (Fast Fourier Transform), IFFT(Inverse Fast Fourier Transform), FPGA(Field Programmable Gate Array).*

Date of Submission: 28-02-2020 Date of Acceptance: 15-03-2020

I. Introduction

Reconfigurable computing is a computer architecture, which combines software with the high performance hardware by very flexible high speed computing fabrics like fieldprogrammable gate arrays (FPGAs).This reconfigurable platform is now being used for designing and implementing SoC due to its low cost and high capacity and tremendous speed [1]. Designing various modern communication standards require digital signal processing throughput. Modeling theses standards on general purpose CPUs can be extremely slow with traditional software. Besides this, for some real time applications the test time can become even longer when noise or real time disturbances are considered. By transferring the processing technique to FPGAs, test time can be reduced significantly and real time application could be implemented. By using large amount of parallel processing, FPGAs can be targeted and reconfigured to test any communication system like OFDM scheme. In present, the application of FPGAs to speed up computation tasks has been researched widely.

Some of these researches have focused on the benefits of using FPGAs for communications processing [2-5]. We have implemented an optimized 8-point FFT or IFFT processor for OFDM system in the FPGA platform using Verilog HDL. A. OFDM System Overview the Orthogonal Frequency Division Multiplexing (OFDM) is developed to support high data rate and can handle multi carrier signals. Its specialty is that, it can minimize the Inter Symbol Interference (ISI) much more compared to other multiplexing schemes [6]. It is more likely improved Frequency Division Multiplexing (FDM) as FDM uses guard band to minimize interference between different frequencies which wastes a lot of bandwidth. But OFDM does not contain inter-carrier guard band which can handle the interference more efficiently than FDM. So, this is the perfect choice for WiMAX as it can help to satisfy the requirements of efficient use of spectrum and minimize the transmission cost [10].

The Discrete Fourier Transform (DFT) is the novel technique to transmit the FDM signal [9]. In OFDM, two digital signal processing algorithm Fast Fourier transform (FFT) and Inverse Fast Fourier Transform (IFFT) are mainly involved. However, the main constraints nowadays for FFT processors used in wireless communication systems for OFDM are execution time and lower power consumption [11]. The main issue in FFT/IFFT processors is complex multiplication, which is the most prominent arithmetic operation used in FFT/IFFT blocks. By using The Cooley–Tukey FFT algorithm, the complexity can be reduced to O (N.log2N) [13]. The main objective of this work is to design an OFDM Transmitter and Receiver using FPGA.

FFT or IFFT are the main building blocks of OFDM, which operates on finite sequences. The OFDM signal is generated by implementing the Inverse Fast Fourier Transform (IFFT) at the transmitter and Fast Fourier Transform (FFT) at the receiver side. Firstly we derive an algorithm for the IFFT and FFT. A variable may correspond to a wire or a register depending on its application and sometimes an operator can be mapped to hardware like adder, latches, multiplexers etc.

II. Implementation Of An 8-Point Fft/Ifft Processor

The implementation of IFFT and FFT is simple as compared to DFT and its 8-point DIF output is derived from the input directly. Multiplication of the twiddle factor is skipped to avoid redundancy and reduce computation time. Thus, IFFT and FFT implementation is optimized. The Fig. 1 shows the 8-point IFFT computation. There are three stages. In stage 1 the input data is accepted directly. The outputs of Stage 1 are feed as the inputs of the Stage 2. In stage 2 computations take place and this process repeats at the final stage 3. The complexity of the output equations increases as the Stage number increases because twiddle factor computations are involved. It includes multiplication and additions operations.

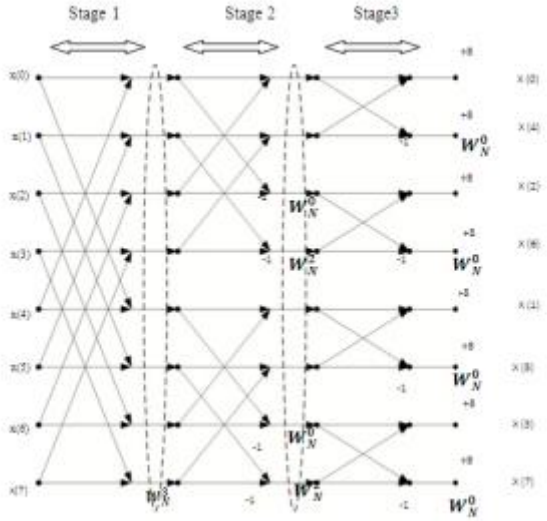

Fig.1 Stage 3 Computation Flow Chart of an 8-point IFFT Computation

Fig. 2 shows an 8-point IFFT block diagram and their interconnections. This module passes the inputs to the submodules that process the IFFT computations. The Pass module consists of 8 D type flip-flop registers. The function of Path 0 and Path 4 is to compute and display the result of these computations. The arithmetic operation for Xout(0) is summation. The Xout(4) involves summation, subtraction and division. The arithmetic operation for Xout(2) and Xout(6) involves real and imaginary operation. They are performed separately. The twiddle factor for this output is either j or –j which contributes to the imaginary components for this path.

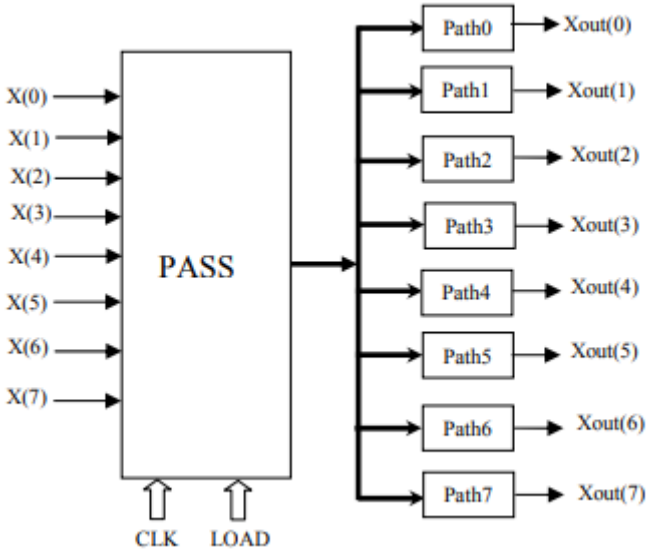

Fig. 2 Block diagram of an 8-point IFFT processor

III. Proposed Architecture:

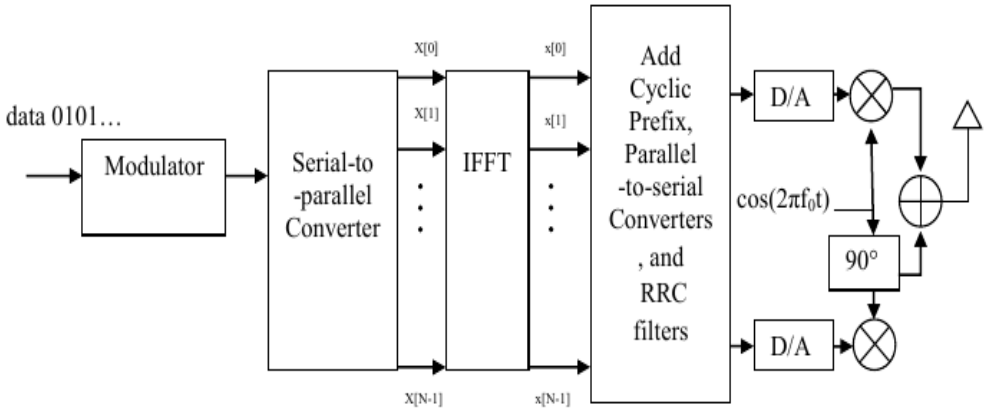

Fig.3.Overall architecture of the OFDM transmitter

Fig.3. shows the overall architecture of the OFDM transmitter. The transmitter ofOFDM is composed of a modulator, a serial-to-parallel converter, an N-point IFFT, two parallel-to-serial converters, and two root raised cosine filters. The data is first modulated by amodulator.

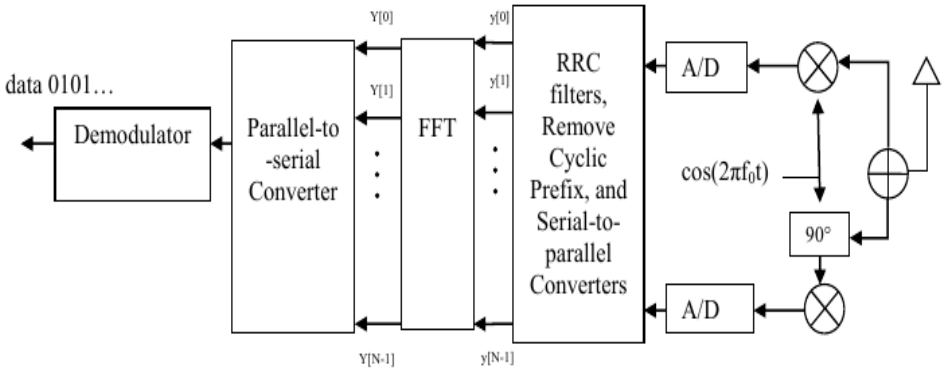

Fig.4. Overall architecture of the OFDM Receiver

Figure.4. shows the overall architecture of the OFDM receiver. The receiver of OFDMcomposes a demodulator, a parallel-to-serial converter, an N-point FFT, two serial-to-parallel converters, and two root raised cosine filters. The received data is first separate into two parts: one is real number and the other is imaginary number. Each of these parts goes through an analog to digital converter and a RRC filter, and then the cyclic prefix is removed. Once these frequency domain data goes through parallel to serial converter, a demodulator is used to demodulate the serial data and recover the original data.

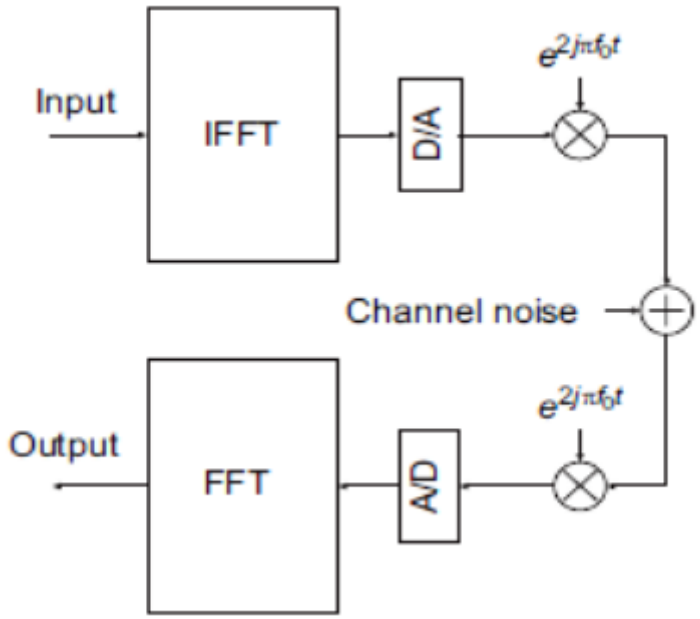

Fig.5. OFDM system based on FFT.

The IDFT can be computed efficiently by Inverse Fast Fourier Transform (IFFT)algorithm. Hence the OFDM modulator can be implemented with one IFFTprocessor and baseband modulator for N subcarriers instead of N modulators forconventional MCM. In similar way, the OFDM demodulator can be implementedmore efficient than that of conventional MCM. The simplified OFDM system based on the FFT is shown in Fig.5.

IV. Performance Considerations And Analysis Of Results

In order to quantify the power savings achieved by specific design choices during the development of the project, power usage simulations were performed at specific project milestones. These milestones include the completion of the2048 point floating point FFT processor, the complete restructuring of theprocessor to use fixed point number representation, the completion of thedynamically reconfigurable FFT processor, and the bypassing of unnecessarymultiplication and addition operations.XilinxXPower Analyzer was used to perform the power analysis of theprocessor once the design was synthesized, mapped, placed and routed by theXilinx ISE design software. The XPower Analyzer is a tool capable of performingmeaningful power simulations on designs prior to final hardwareimplementations. In the case of this project, default switching and timing settingsfor the simulations were used to assess power performance independent ofactual inputs or FFT size. The actual power performance of an FFT processorwill vary with size as the amount of processing done in each component does notremain constantly proportioned with varying FFT input size. A brief discussion ofthe optional use of timing and switching constraints for power simulations isincluded in the further research section of this report.

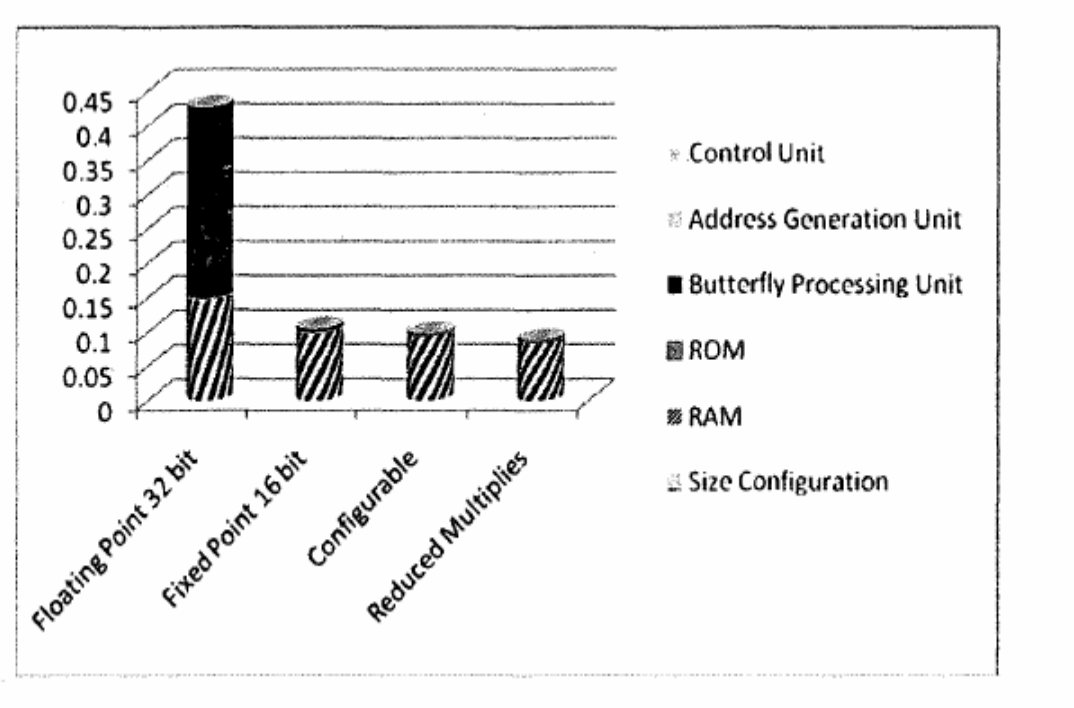

Fig.6.FFT processor power (W) comparison

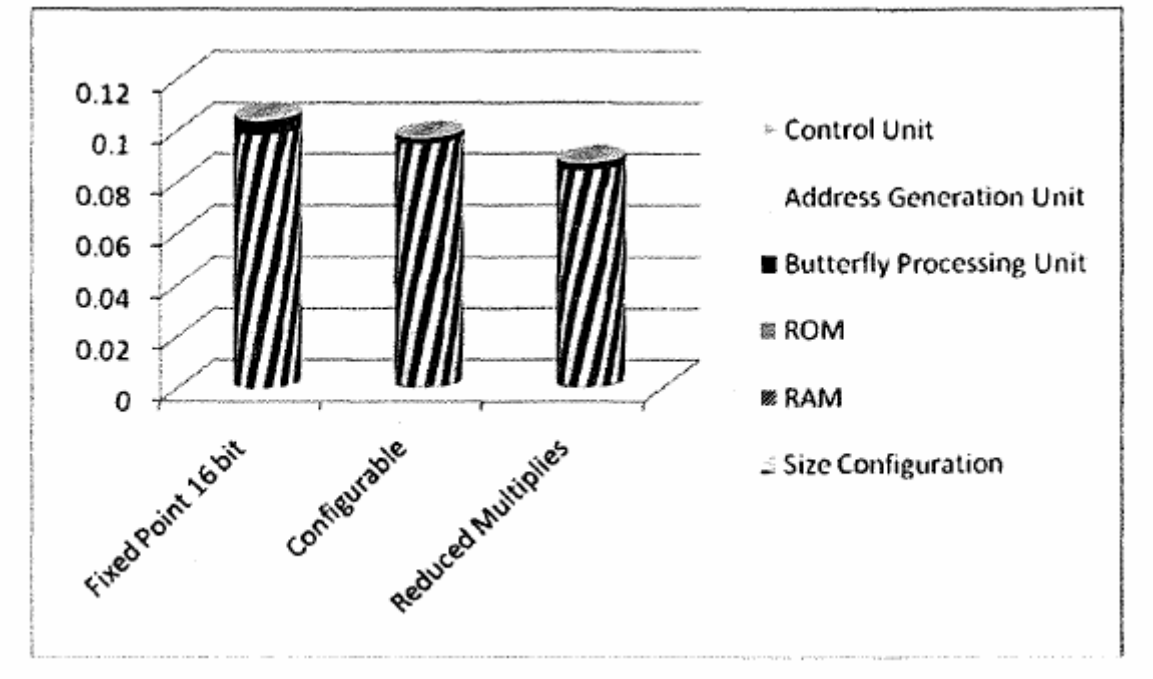

Fig.7. Fixed point FFT processor power (W) comparison

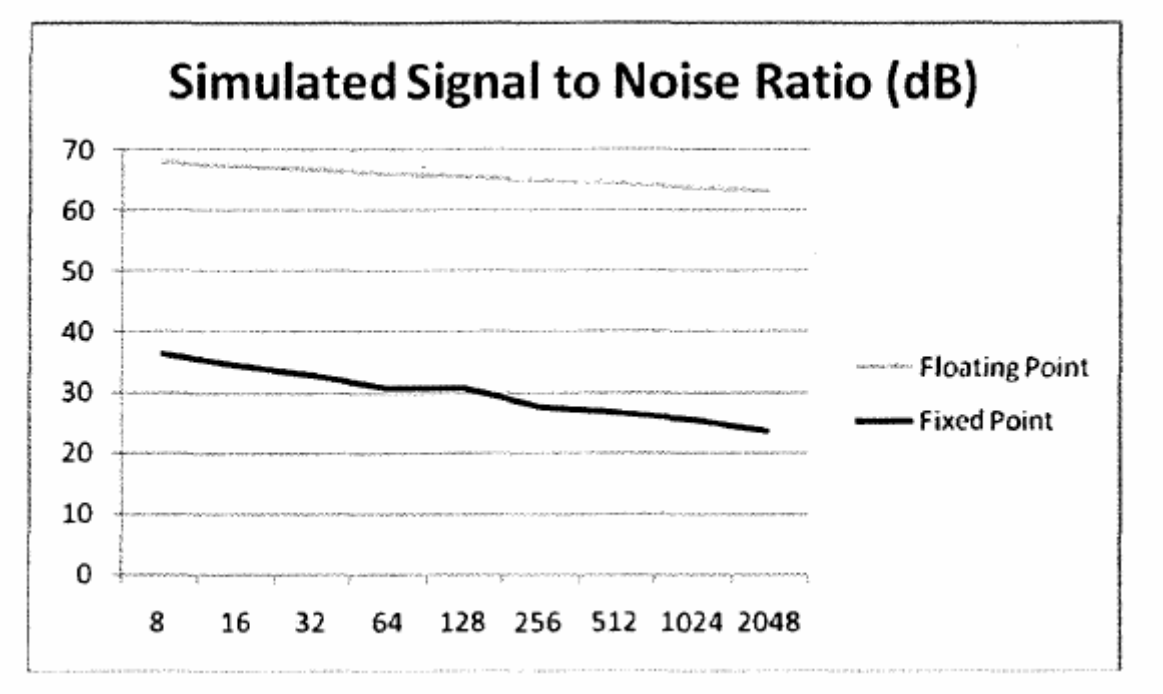

Fig.8.Signal to noise ratio comparison

There is approximately a 30dB difference between the two processors, so while significant savings were made on power, they were paid for by the output output SNR. If a particular application demands that higher SNR values be achieved, this can be manipulated by increasing the data path width in the processor design. Less significant improvements can also be achieved by employing more aggressive or sophisticated rounding and overflow detection in the fixed point operations of the processor.

V. Simulation Results

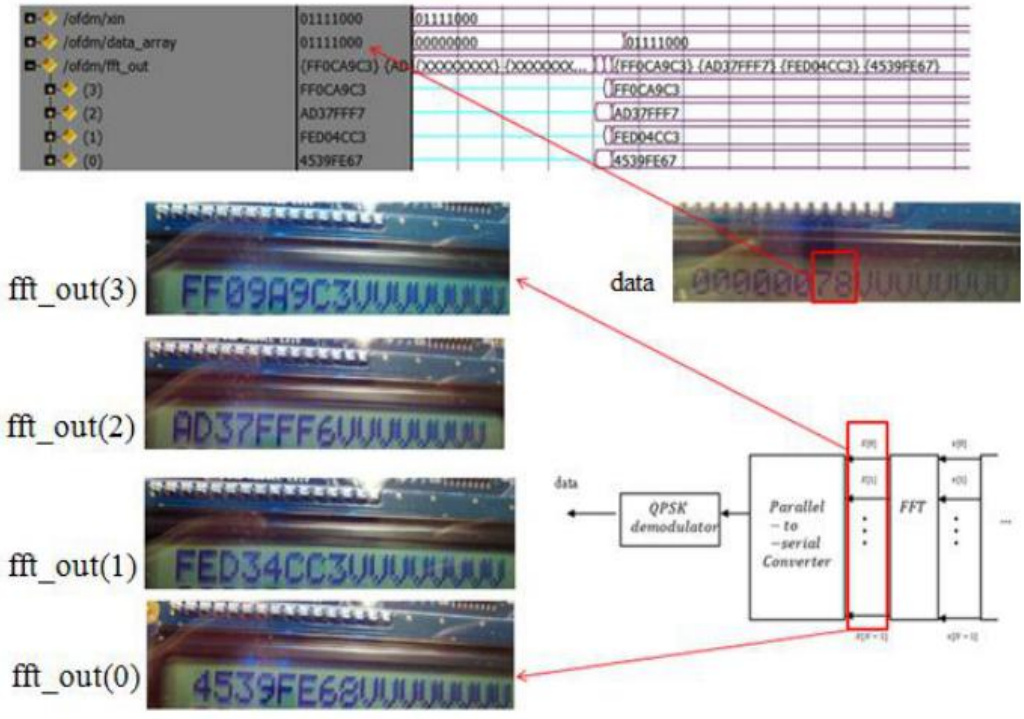

Fig.9.Simulation Results In both FPGA kit and ModelSim.

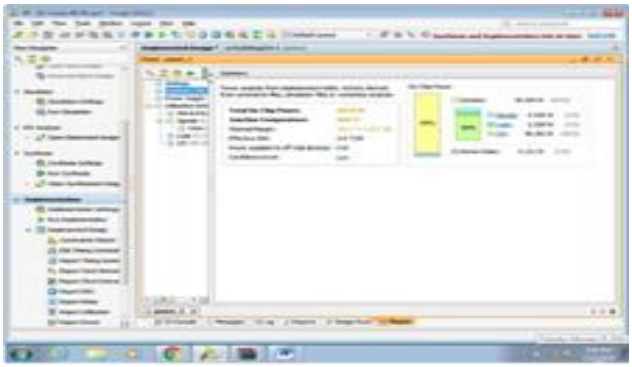

Fig.10.Shows the power report of proposed architecture.

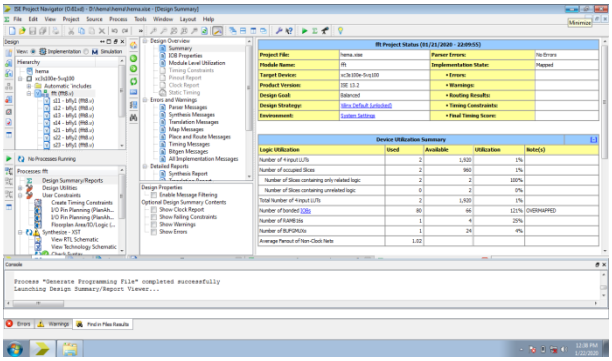

Fig.11.Shows the Area report of proposed architecture.

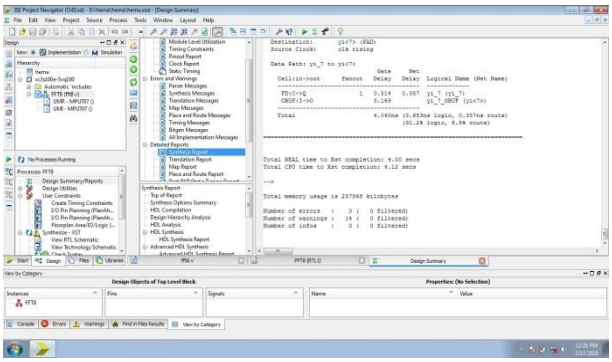

Fig.12.Shows the Delay report of proposed architecture.

VI. Conclusion

This project considers numerous power-saving techniques available for FFT processor design while taking into account the current technology requirements that are emerging for tomorrow's communications. As performance requirements continue to increase while devices are becoming more and more portable, the need for power efficiency becomes ever more important. This project reviewed several possible design decisions and ultimately selected specific methods for implementation in the FFT processor. It was decided to implement the FFT processor on an FPGA platform because of the benefits associated with this technology. Compared to a Digital Signal Processing (DSP) microprocessor, FPGAs can easily outperform a DSP in computations per cycle and require far less power to run. When compared to an Application Specific Integrated Circuit (ASIC), the power consumption could actually be greater in many instances. Where the FPGA has advantages over the ASIC is in the ability to quickly develop, test, change, and customize the design again and again. Development time is faster and the ability to modify the design in the future to integrate it into a larger system or meet the requirementsof changing technologies is invaluable. ASIC makes sense for high volumeproduction and has some performance and power advantages, but with FPGA'sability to be reprogrammed and modified on the fly, it was determined as thechoice of implementation for this project.

References

[1]. J. Mitola and G. Q. Maguire, "Cognitive radio: making software radios more personal," IEEE Personal Communications, vol. 6, no. 4, pp. 13-18, Aug. 1999.

[2]. B. Fette, "SDR Technology Implementation for the Cognitive Radio,"presented at Cognitive Radio Technologies Proceeding, Washington, D.C.,2003.

[3]. Q. Zhang, A. B. J. Kokkeler, and G. J. M. Smit, "An efficient FFT for OFDM based cognitive radio on a reconfigurable architecture," in ICC 2007 Proceedings, 2007, pp. 6522-6526.

[4]. M. Sherman, A. N. Mody, R. Martinez, and C. Rodriguez, "IEEE standards supporting cognitive radio and networks, dynamic spectrum access, and coexistence," IEEE Communications Magazine, pp. 72-79, Jul. 2008.

[5]. J. Benko, et al, "Draft PHY/MAC specification for IEEE 802.22," Institute of Electrical and Electronics Engineers, IEEE 802.22-06/0069M, 2006.[Online]. Available: https://mentor.ieee.org [Accessed: Aug. 3, 2008].

[6]. C. H. Su and J. M. Wu, "Reconfigurable FFT design for low power OFDM communication systems," Institute of Electrical and Electronics Engineers, 2006. [Online]. Available: http://ieeexplore.ieee.org [Accessed: Jun. 23,2008].

[7]. C. J. Kim, M. S. Song, G. Z. Ko, S. H. Hwang, and J. S. Urn, "OFDMA PHY parameters for WRAN system," Institute of Electrical and Electronics Engineers, IEEE 802.22-07/0189r0, 2007. [Online]. Available: https://mentor.ieee.org [Accessed: Aug. 3, 2008].

[8]. "Orthogonal frequency-division multiplexing," in Wikipedia the Free Encyclopedia, 2008. [Online]. Available: Wikipedia, http://en.wikipedia.org [Accessed: Aug 1, 2008].

[9]. J. Tian, Y. Xu, H. Jiang, H. Luo, and W. Song, "Efficient algorithms of FFTbutterfly for OFDM systems," in IEEE 6th CAS Symposium on Emerging Technologies: Mobile and Wireless Communication, 2004, pp. 461-464.

[10]. S. Y. Lee and C. C. Chen, "VLSI implementation of programmable FFT architectures for OFDM communication system," in IWCMC proceedings, 2006, pp. 893-898.

"Desigin of Ofdm Transmitter and Reciever with Programmable Fft" International Journal of Engineering Science Invention (IJESI), Vol. 09(03), 2020, PP0 09-16.