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Simulation of A H Bridge Multilevel Inverter and its comparison with conventional H bridge Multilevel Inverter

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***Abstract*—*In this paper, a new asymmetric topology based on cascaded H-bridge has been proposed which can generate a output voltage of 19 level using a very less component. The proposed basic unit is asymmetric in nature. It can produce the given levels by using only 12 unidirectional power switches and 3 dc sources of magnitude V, 3V, 0.5V. It is capable of generating both integral and fractional output levels .The basic unit is connected symmetrically in a cascade manner. Proposed topology is compared with other MLI topologies that have been recently developed in terms of number of switches, gate driver circuits, diodes and dc link. It is observed that this topology uses less number of components at a given level among in comparison to other topologies. Simulation of the proposed basic unit is done in MATLAB/SIMULINK. The circuit is verified for different load conditions such as R-L, L and sudden load change conditions. Total Harmonic Distortion of both output current and output voltage is also determined. This topology is found to generate output levels with very low Total Harmonic Distortion.*

Keywords*—*asymmetric;cascaded H-bridge; total harmonic distortion; voltage level

I. Introduction

Nowadays, the application of multilevel inverter (MLI) increases significantly in different fields such as motor drive applications, renewable energy conversion systems, electric vehicle, UPS system etc due to its inherent features [**1**]-[**4**]. MLI generates staircase output voltage waveform from capacitive sources or multiple dc sources. Due to the staircase nature of the output waveform, the quality of output waveform improves and follows the near sinusoidal nature. As compared to classic two level inverters MLI has a number of benefits such as it gives improved output voltage waveform, Lower stress voltage across switch, More power handling capacity, Lower electromagnetic interference, Lower output filter size.

The classic multilevel inverter topologies are cascaded H-bridge (CHB), Diode clamped, Flying capacitor (FC). The basic version of CHB MLI come in the year of 1975 [**9**]. After that in 1981, the diode clamped MLI came into existence [**5**]-[**6**]. After one decade 1991, the flying capacitor MLI has been introduced [**7]-[8**]. In diode clamped MLI, the input voltage is split into multiple lower voltage level by capacitor bus. The different switch voltages are clamped through the diode. This inverter is very popular in industrial application due to its simple structure but above three level of output voltage, the structure requires large number of clamping diodes. Further the capacitor voltage balancing is becomes very complex as the level of inverter increase. Flying capacitor is more flexible in nature compared to DCM MLI unlike DCM, FC clamped the switch voltages by flying capacitor. This structures requires large number of flying capacitor as the output voltage level increase more than three. CHB generates multilevel output voltage waveform by adding or subtracting different dc voltage sources. This topology does not require any clamping diodes or flying capacitors. The topology is modular in nature and simple in structure but the topology requires a large number of isolated dc sources as the output voltage level increase.

To mitigate the different limitations of classical multilevel inverter topologies, the researchers are introducing different new structures of MLI in recent years. The topological improvement of classical MLIs are becomes an interesting and hot research area in the field of power electronics.

In paper [**10**], a new arrangement of cascaded MLI has been presented. The main advantage of this topology is that it uses only unidirectional switches to generate a particular level. Therefore, it uses of less quantity of components like IGBTs and driver circuits. The downside of this topology is that the stress voltage across switches is more. In paper [**11**] another new arrangements of cascaded MLI has been employed. The limitations of this topology is that only symmetric source configuration can be employed. So, to generate higher number of levels it requires more number of dc links. In paper [**12**] an asymmetric type MLI is presented which uses ten unidirectional switches to only generate nine output voltage level. So, for given voltage level this topology has high device count. This topology also incurs high switching losses. As this topology possess high

THD the cost requirements of filters is high. In paper [**13**], multiple number of sub-multilevel units are connected to provide a novel cascaded MLI. This topology encounters the same disadvantage of increased device count with increasing number of levels. Paper [**14**] presents a novel sub-module MLI to which trinary source configuration is implemented in order to generate 17 output voltage levels. However, to generate the voltage the output levels it uses four dc sources along with unidirectional and bidirectional switches. Hence the number of components increases with increase in number of levels.

A novel asymmetric MLI topology is introduced which uses unidirectional switches to generate output voltage levels. The sole objective of this topology is to reduce the component count as the number of level increments. Section I comprises of the literature survey of the MLI topologies that have been recently developed. Section II introduces the basic unit of the proposed topology. In Section III, cascade connection of the proposed basic unit is presented. Comparison study is performed in Section IV followed by simulation study in Section V. Section VI contains the conclusion.

II. Basic Unit of Proposed Topology

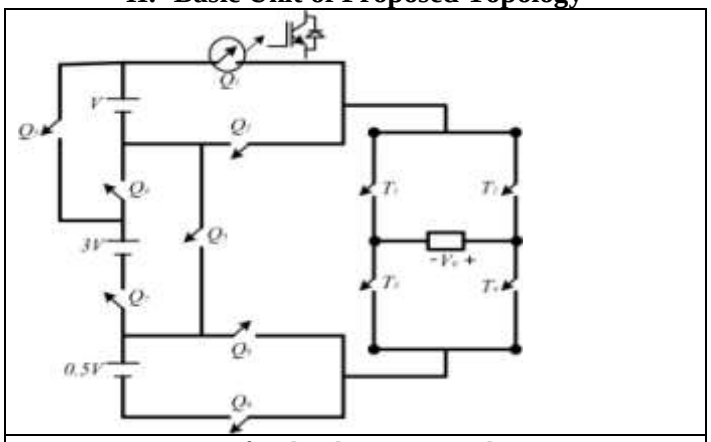


Fig. 1. Basic unit of 19 level inverter topology

Fig. 1 presents the basic unit of the proposed topology. It consists of 12 unidirectional switches i.e. Q_1, Q_2, Q_3, Q_4, Q_5, Q_6, Q_7, Q_8, T_1, T_2, T_3, T_4. The basic unit makes use of dc sources of three different varieties i.e. $0.5V_{dc}$, $1V_{dc}$, $3V_{dc}$. Among the switches (Q_1, Q_2), (Q_3, Q_4), (Q_6, Q_8), (T_1, T_2) and (T_3, T_4) are complimentary pairs and thus do not turn ON/OFF simultaneously. The basic unit has the capability to produce 19 output voltage levels. The hallmark of the proposed basic unit is that it has the ability to produce fractional voltage levels. Switches T_2 and T_3 helps in generating positive voltage levels whereas T_1 and T_4 are utilized to produce negative output voltage levels. The zero level can be generated either by turning ON T_1 and T_2 or T_3 and T_4.

Table I presents the overall idea about the different voltage levels that can be generated and the corresponding switches that are operated. The switches which are turned ON are indicated by '1' whereas '0' indicates that the respective switch is turned OFF while generating a particular output voltage level. In order to generate a particular output voltage level minimum of five switches are operated in the basic unit. In Fig 2(a) shows the current flow path in the basic unit while producing an output voltage of 0.5V. Whereas red line represents the direction for flow of current. Fig 2(b) shows the current path corresponding to 2V where six switches (Q_2, Q_3, Q_7, Q_8, T_1, T_4) are switched ON. Similarly Fig 2(c), 2(d), 2(e), 2(f), 2(g) and 2(h) depict the current flow path corresponding to the output voltages 2.5V, 4.5V, -0.5V, -2V, -2.5V and 4.5V respectively.

TABLE I. SWITCHING TABLE

Output Voltage levels	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	T_1 T_4	T_2 T_3
$+4.5V_{dc}$	1	0	0	1	0	1	1	0	0	1
$+4V_{dc}$	1	0	0	1	0	0	1	1	0	1
$+3.5V_{dc}$	0	1	0	1	0	1	1	0	0	1
$+3V_{dc}$	0	1	0	1	0	0	1	1	0	1
$+2.5V_{dc}$	0	1	1	0	0	1	1	0	0	1
$+2V_{dc}$	0	1	1	0	0	0	1	1	0	1
$+1.5V_{dc}$	1	0	0	0	1	1	0	0	0	1
$+1V_{dc}$	1	0	0	0	1	0	0	1	0	1
$+0.5V_{dc}$	0	1	0	0	1	1	0	0	0	1
$0V_{dc}$	0	0	0	0	0	0	0	0	0	1
$-0.5V_{dc}$	0	1	0	0	1	1	0	0	1	0

$-1V_{dc}$	1	0	0	0	1	0	0	1	1	0
$-1.5V_{dc}$	1	0	0	0	1	1	0	0	1	0
$-2V_{dc}$	0	1	1	0	0	0	1	1	1	0
$-2.5V_{dc}$	0	1	1	0	0	1	1	0	1	0
$-3V_{dc}$	0	1	0	1	0	0	1	1	1	0
$-3.5V_{dc}$	1	0	0	1	0	0	1	1	1	0
$-4V_{dc}$	1	0	0	1	0	0	1	1	1	0
$-4.5V_{dc}$	1	0	0	1	0	1	1	0	1	0
Switching transitions in each cycle	6	8	4	2	4	16	3	14	1	1

III. Proposed Cascaded MLI Topology

This section discusses the proposed MLI structure. The proposed topology consists of m segments of proposed basic unit connected in cascade configuration. The output voltage level of the proposed topology can be expressed as follows.

$$V_0(t) = V_{01}(t) + V_{02}(t) + \cdots V_{0m}(t) \quad (1)$$

where $V_{01}(t)$, $V_{02}(t)$ ..... $V_{om}(t)$ are the output voltage of segment I, segment II,....., segment m respectively. In order to facilitate high output voltage levels along with less voltage stress across the switches. The segments are cascaded in a symmetric manner. The advantages of this topology is it's modular structure and the sense of reliability. If overload condition or any fault condition damages any segment, then also the proposed topology is capable of producing output with reduced voltage levels. Fig.3 represents the diagram for cascaded structure for proposed topology.

If m equals to the number of segments taken into consideration it can be then it can be represented in terms of number of levels (N_L) as follows:

$$m = \frac{N_L - 1}{18} \quad (2)$$

Table II provides the number of switches, number of drivers, number of dc links and TSV of the proposed topology expressed in terms of m and N_L.

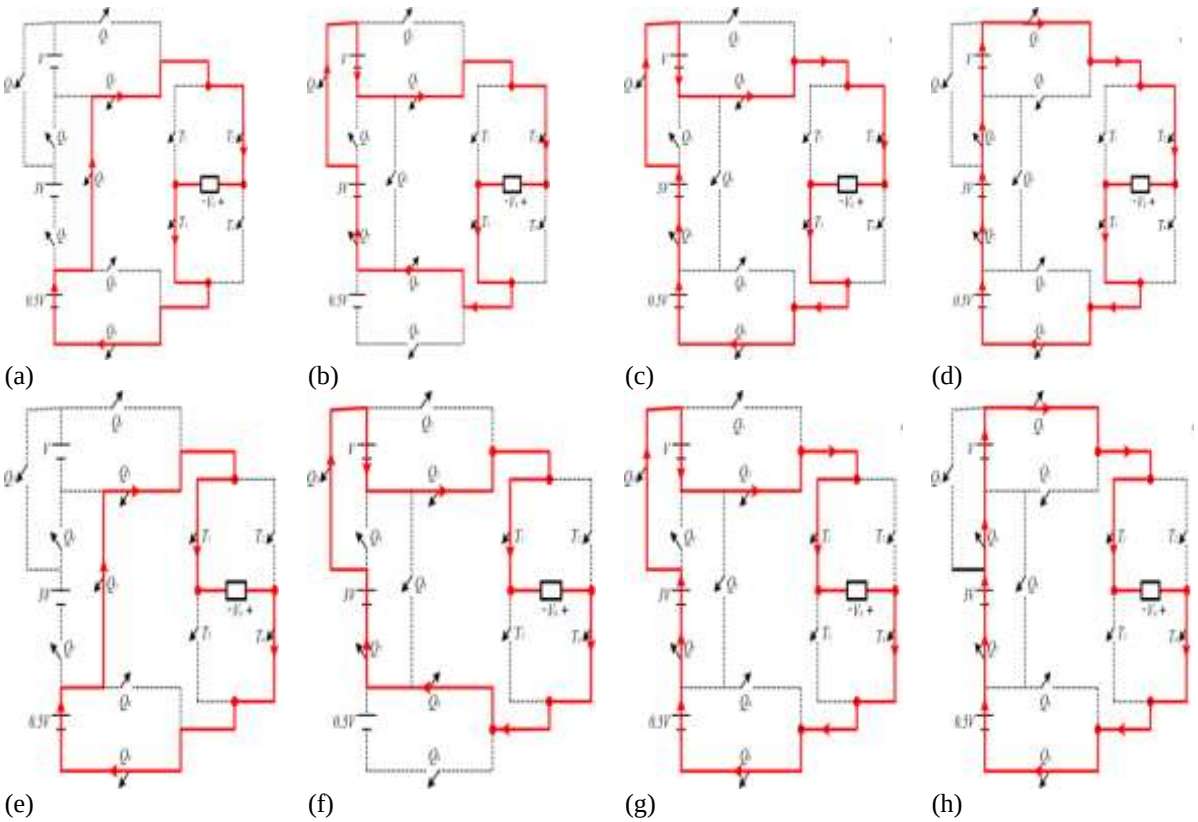


Fig. 2. Current path for generating (a)$0.5V_{dc}$ (b)$2V_{dc}$ (c)$2.5V_{dc}$ (d)$4.5V_{dc}$ (e)$-0.5V_{dc}$ (f)$-2V_{dc}$ (g)$-2.5V_{dc}$ (f)-

$4.5V_{dc}$

TABLE II. TABLE STYLES

Table Head	**Based on number of module units**	**Based on number of desired levels**
Switches	12m	$\frac{2}{3}(N_L - 1)$
Driver circuits	12m	$\frac{2}{3}(N_L - 1)$
DC Links	3m	$\frac{1}{6}(N_L - 1)$
TSV	28m	$\frac{14}{9}(N_L - 1)$
Vmax	4.5m V_{dc}	$\frac{1}{4}(N_L - 1)$ V_{dc}

IV. Comparison Study

Comparison study has been performed in this section with the MLI topologies mentioned in **[10-14]**. The basic unit of the proposed topology is examined thoroughly and is compared with the above-mentioned topologies in terms of number of switches(N_{switch}), dc links($N_{dc\ link}$), driver circuits(N_{driver}) and TSV. Fig. 4(a) shows graphical representation of comparison between number of switches among different topologies and proposed topology for a given range of voltage levels. It can be observed that the proposed topology utilizes least number

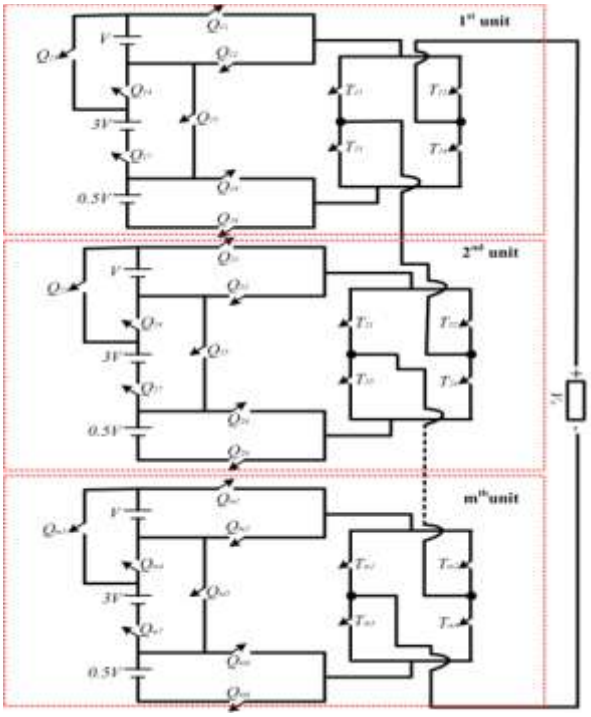
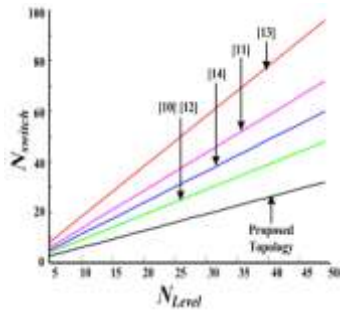
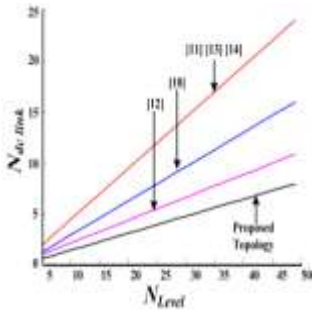


Fig.3 Cascade connection of proposed topology

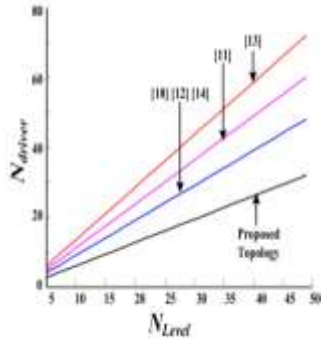
of switches to generate a particular level. From fig. 4(b) provides the comparison of the topologies in terms of dc links and it can be seen that the proposed topology requires least number of dc links among other topologies. Fig. 4(c) represents the comparison of number of driver circuits utilized by certain topology for generating specified number of voltage levels. Similarly fig. 4(d) represents the comparison of number of diodes utilized by the circuit for particular output voltage level and it can be seen that the proposed topology requires least number of diodes.



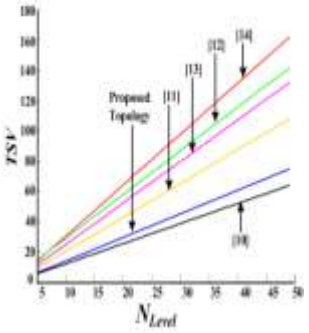
4(a)



4(b)



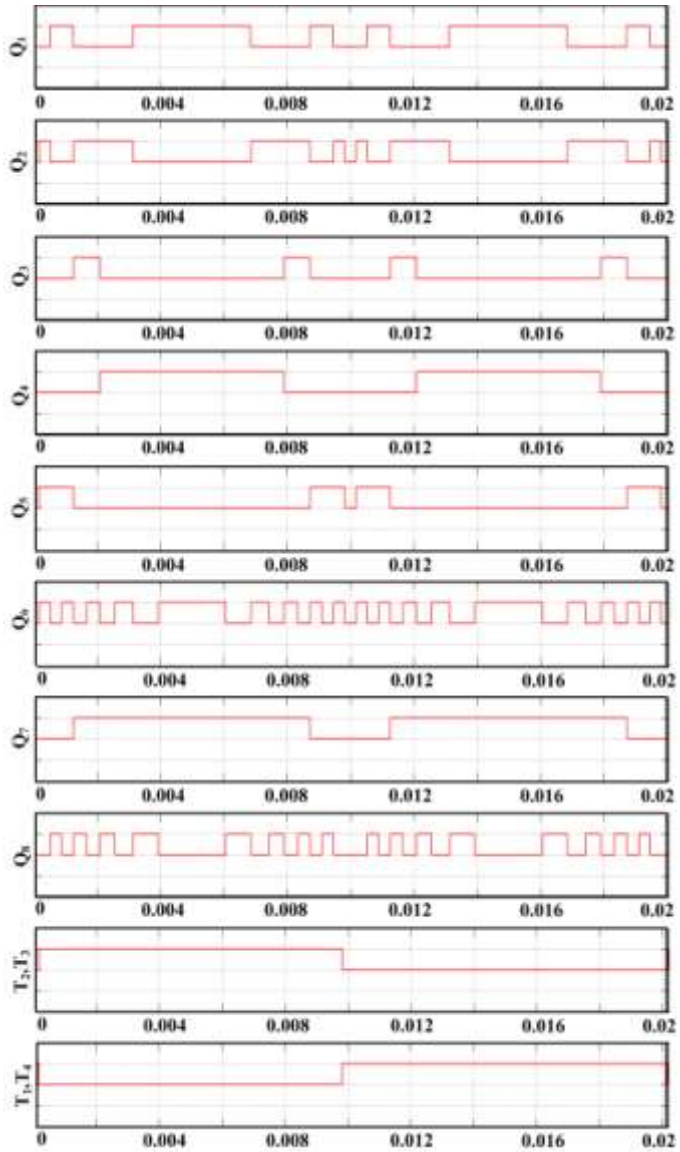
4(c)



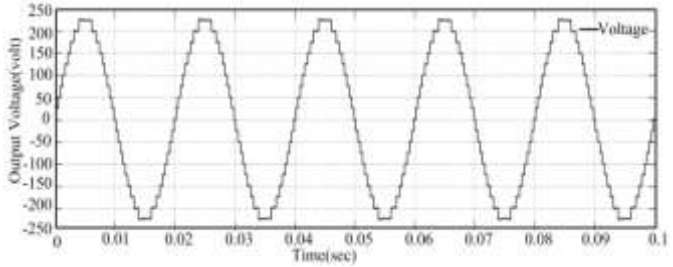
4(d)

V. Simulation Study

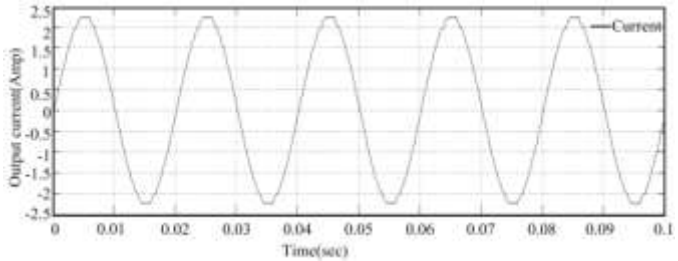
In this section, the basic unit of the proposed topology is analyzed and simulated in MATLAB/SIMULINK. Different load conditions are taken into consideration to check the efficacy of the circuit. Fig.5 represents gate pulses that is applies across each switches for given cycle. Fig. 6 shows the simulation waveform of the basic unit capable of generating 19 levels. Fig. 6(a) represents the output voltage waveform under R-L load condition where resistance and inductance is considered to be 100Ω and 25mH respectively. Fig 6(b) represents the output current waveform under the R-L load condition. The value of maximum current is found to be 2.3 A. In fig 6(c) and 6(d) the FFT analysis of the output voltage and output current are shown respectively. The THD for output voltage is 4.33% and that of output current is 1.60%. Fig 6(e) represents the output voltage and current waveform under L load condition where L=125mH. It can be observed that the current waveform is sinusoidal and it lags the output voltage by a margin of 90 degrees. Fig 6(f) represents the output voltage and current waveform under sudden load change condition. In this case the load is suddenly changed in between 100Ω and 50Ω and the variation in the output voltage and current waveform is noted. Firstly, the load was considered to be at 100Ω. When the load is suddenly changed to 50Ω, the output current increases. On the other hand, when the load is changed from 50Ω to 100Ω a drop is the load current is noticed. It is to be noted that the sudden change in load does not affect the output voltage waveform.



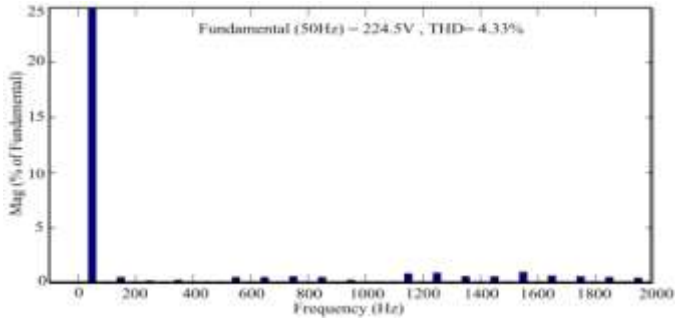
Switching state



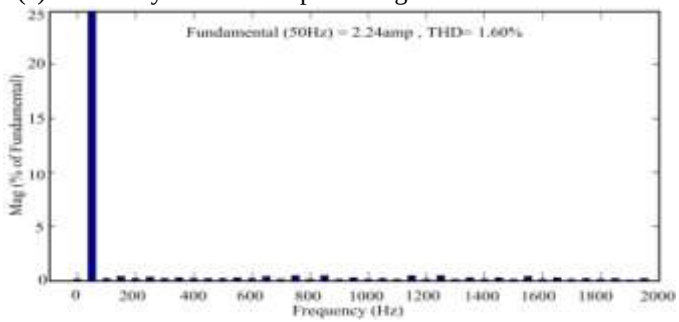
6(a) output voltage waveform under R-L load



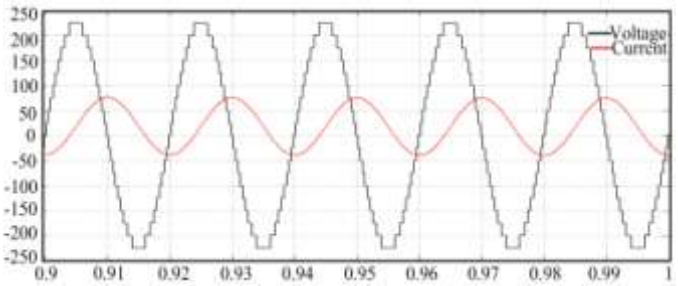
6(b)output current waveform under the R-L load



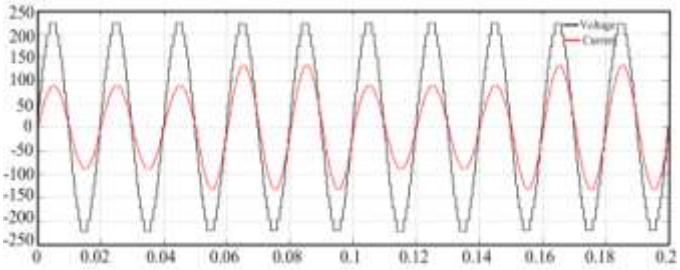
6(c) FFT analysis of the output voltage



6(d) FFT analysis of the output current



6(e)output voltage and current waveform under L load



6(f) output voltage and current waveform under sudden load

VI. Conclusion

A Novel MLI topology is proposed. The topology is capable of generating 19 levels and it can produce both integral and fractional output voltage levels. Cascade connection of the proposed basic unit is presented and the mathematical expressions regarding the number of switches, driver circuits and dc links it employs for generating a particular voltage level is also mentioned. A thorough comparison study is performed with other topologies and it is found out that the proposed topology satisfies it's sole objective of reducing the device count by using least number of components in comparison to other topologies. Simulation studies shows the output voltage and current waveform under R-L, L and sudden load change condition. The THD for output voltage and output current under R-L load condition was found to be 4.33% and 1.60% respectively. Since this topology utilizes three different varieties of sources, this topology can be applicable in renewable energy conversion systems.

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