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Design of Roba Mutiplier Using Booth Signed Multiplier and Brent Kung Adder

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Abstract : *Approximate Circuits Are Becoming An Effective Solution To Co Accurately Operating Circuits If Energy Efficiency Is Concerned And The Application Is Error Tolerant. In This Paper An Approximate Multiplier Which Is Based On Rounding Is Designed Using Booth Signed Multiplier And The Brent Kung Adder. The Brent Kung Adder Is One Of The Parallel Prefix Adder Which Greatly Reduces The Consumption Of Area For Higher Order Bits. Booth Sign Multiplier Is Used For Intermediate Multiplication Process Which Greatly Reduces The Delay When Compared To Other Multipliers. This Proposed Approximate Multiplier Has Less Delay And Consumes Less Area And Its Efficiency Is Compared With Those Some Of Previous Approximate And Accurate Multipliers In Terms Of Power, Area And Delay.*

Keywords - *Approximate Multiplier, Booth Sign Multiplier, Brent Kung Adder, Less Area, High Efficient.*

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I. INTRODUCTION

In Most Of The Vlsi Circuits The Energy And Area Minimization Are The Main Design Requirements In Order To Achieve High Speed And High Efficient Electronic Systems Especially The Portable Ones Such As Smart Phones, Tablets, And Different Gadgets. Digital Signal Processing (Dsp) Blocks Are The Main Component Of These Portable Devices For Realizing Various Multimedia Applications. The Multiplication Operation Has The Greatest Share Among All Arithmetic Operations Performed In These Dsp Systems. Therefore, Improving The Various Design Parameters Of Multipliers Will Increase The Efficiency Of Processors. It Is Found That In Some Applications Like Image And Video Processing, The Results Obtained From The Arithmetic Operation With Small Errors Do Not Affect The Performance Or Functionality Of The System. The Approximate Circuits Are Becoming An Alternative Solution To Increase The Efficiency Of The Circuits If Energy Efficiency Is Concerned And Target Application Is Error Tolerant. This Is Applicable To The System Or Circuits That Are Mainly Composed Of Adders And Multipliers.

II. APPROXIMATE MULTIPLIERS

Approximate Multipliers Are The Modified Form Of Some Precised Multiplier Which Are Used In The Application Where The Target Output Is Error Tolerant And The Energy Efficiency Is Highly Concerned. For A Particular Application The Designer Can Approximate Circuits Such As Adders And Multiplier By Applying Some Approximate Computation Methods. This Paper Proposes An Approximate Multiplier Which Is Area And Energy Efficient Constructed Using Booth Signed Multiplier And The Brent Kung Adder. The Booth Signed Multiplier Greatly Reduces The Delay When Compared To Other Binary Multipliers Since It Eliminates The Number Of Partial Products. It Is Applicable For Both Signed And Unsigned Number Multiplication. The Brent Kung Adder Is One Of The Parallel Prefix Adder The Logarithmic Structure Of This Adder Will Leads To Less Area Consumption When Compared To Other Adders. Thus The Proposed Approximate Multiplier Is Designed For The Applications Where The Area And The Minimization Of Energy Is Given A Higher Priority. The Efficiency Of The Proposed Multiplier Is Compared With Some Of The Approximate And Accurate Multipliers Used In The Previous Systems In Terms Of Power, Delay And Area.

III. OPERATION OF APPROXIMATE COMPUTATON

The Approximate Computation Involves Three Multiplication, One Addition And Subtraction Operation As Given In The Equation 1, Which Gives The Approximate Value Of The General Floating Point Multiplication. The Block Diagram For The Approximate Computation Consists Of Four Major Parts Which Are Sign Detector, Rounding Off Block, Booth Signed Multiplier And The Brent Kung Adder.

The Booth Sign Multiplier Is Used For The Multiplication Process And Addition Operation Is Performed By Brent Kung Adder Which Is One Of The Parallel Prefix Adder .Consider The Two Input Values

As C And D Having The Rounded Values As Cr And Dr. The Following Expression Is Used For Performing The Approximate Computation.

$C \times D \qquad Cr \times D + Dr \times C - Cr \times Dr \qquad (1)$

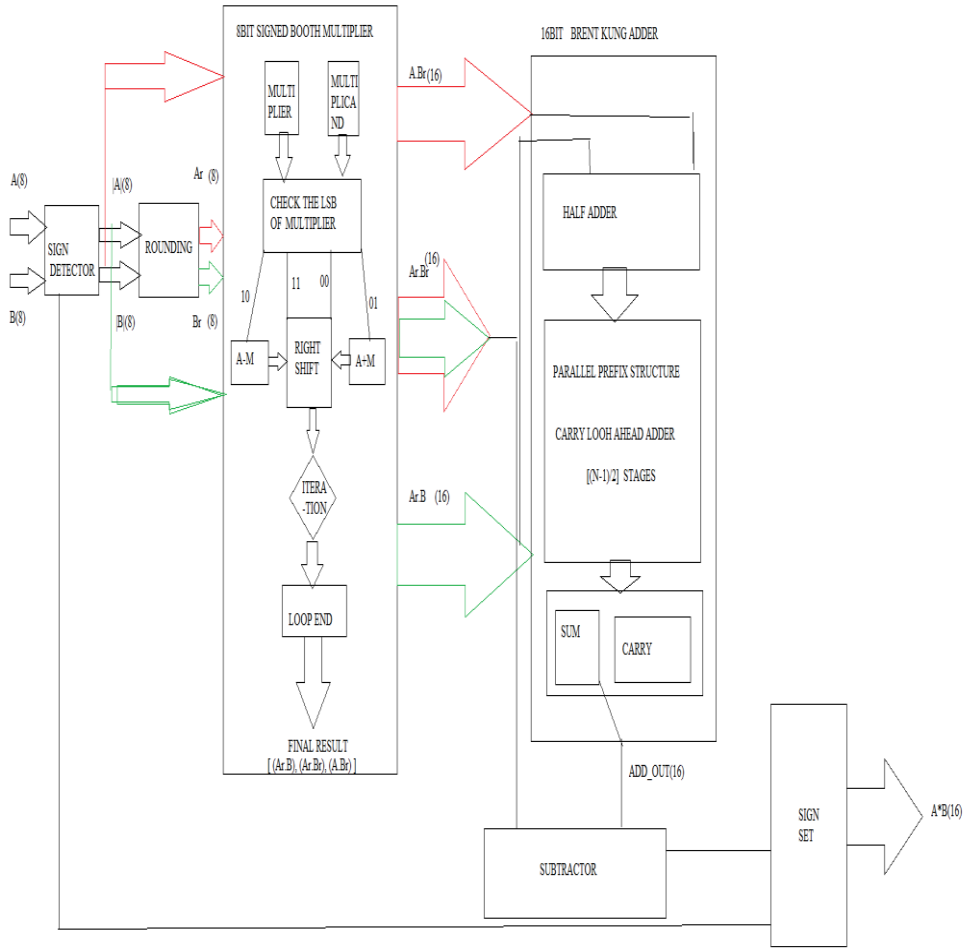

Figure 1: Block Diagram Of Proposed Approximate Multiplier

IV. SIGN DETECTOR AND ROUNDING-OFF OPERATION

The Sign Detector Is Used For Detecting The Sign Of The Input Values, Initially The Input Values Are Converted Into N-Bit Binary Number Then The Msb Bits Of The Input Values Are Extracted And By Applying The Xor Operation The Sign Of The Final Output Value Is Obtained And It Is Forwarded To The Sign Set, The Figure 1 Clearly Shows The Forwarding Of Sign Bit From Detector To The Sign Set. The Msb Bit Of The Output Represents The Sign Of The Output Which Is Determined Using The Sign Set. If The Obtained Msb Bit Is '0' Then The Sign Is Positive, If It Is '1' Then The Sign Is Considered As Negative. After The Rounding Off Block The Rounded Off Values Are Considered As Cr.

V. BOOTH SIGNED MULTIPLIER

The Booth Signed Multiplier Algorithm Is One Of The Best Algorithms As It Treats Both Signed And Unsigned Number Multiplication Uniformly. It Performs Shift And Add Method For The Multiplication Process. In General If Two Numbers Is Getting Multiplied I.E., Multiplier And Multiplicand It Needs More Memory For Storing Its Partial Products. The Main Advantage Of Booth Signed Multiplier Is That It Eliminates The Several Partial Products And Attains The Resultant Product Within Short Span Of Time. This Greatly Reduces The Delay When Compared To Other Conventional Multipliers. It Follows An Algorithm Called As Booth Signed Algorithm Through Which The Multiplication Process Takes Place.

VI. Algorithm

Initialize The Accumulator To Be Zero And Consider Any Two Numbers For Multiplication. For Negative Numbers Two Complement Should Be Taken By 1's Complement And Adding 1 With It. The Comparison Should Be Made With The Lsb Of Multiplier And Multiplicand Bits. The Fig 2, Shows The Flowchart Of Booth Algorithm Through Which The Various Steps Are Followed While Performing The Multiplication Process.

It Possess Following Cases,

Case 1: If The Bit Is 01

Add The Multiplicand With Value Of Accumulator And Perform Arithmetic Right Shift.

Case 2: If The Bit Is 10

Subtract The Multiplicand With The Value Of Accumulator And Perform Arithmetic Right Shift.

Case 3: If The Bit Is 00 Or 11

The Previous Stage Value Should Be Right Shifted And Repeat The Process Until The Count Value Becomes 0.

As Per The Equation 1 The Approximate Multiplication Of Two Floating Point Numbers Is Performed By Three Multiplication, One Addition And One Subtraction Operation. The Three Multiplication Operations I.E., C×Dr, D×Cr , Cr×Dr Are Performed Using Booth Signed Multiplier, Which Is Referred As Fastest Multiplier. These Will Be In The Form Of 8 Bit Binary Number, So That It Is Convenient For The Booth Sign Multiplier To Perform The Multiplication Operation. Since The Booth Sign Multiplier Has The Lowest Delay Than Any Other Multipliers, It Is Used In The Proposed System For Multiplication Purpose To Reduce The Delay. The Output From The Booth Signed Multiplier Will Be 2n- Bit Binary Number Since The Multiplication Is Done Between Two N-Bit Binary Numbers. Thus It Greatly Reduces The Delay By Using Eliminating The Number Of Partial Products, This Leads To Increase In Efficiency Wherever It Is Implemented In An Application.

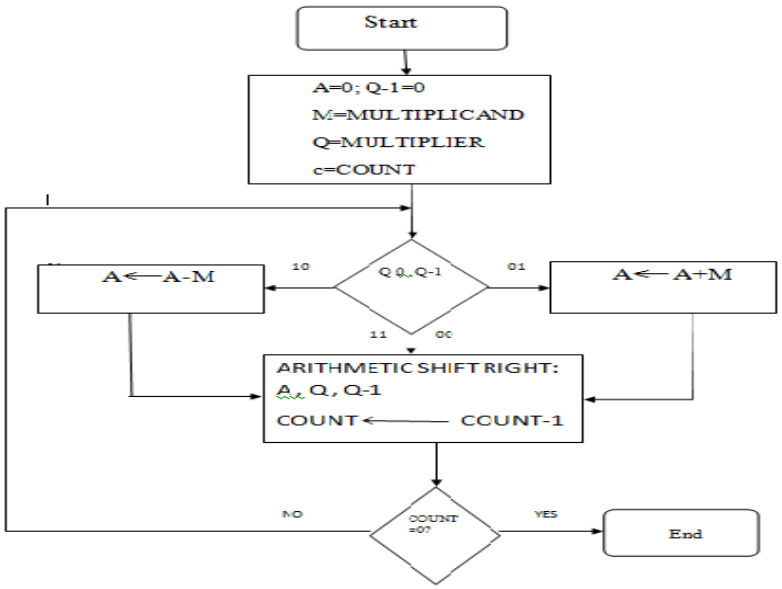

Figure 2: Flowchart For Booth Algorithm

VII. Brent Kung Adder

The Complex Structure Of Any Adder Will Greatly Affects The Speed Of The Circuit. In Order To Increase The Area-Delay Efficiency Many Research And Development Continues To Focus On The Reduction Of Area And Delay Of The Adder. The Parallel Prefix Computational Methods Are Used In Order To Overcome The Problems Faced By Using Ripple Carry And Carry Look Ahead Adder Design. Brent And Kung (Bk) Proposed New Technique For Designing The Parallel Prefix Computation By Modifying The Conventional Parallel Prefix Adders Which Is Mainly Designed To Reduce The Area Of The Adder For The Higher Order Inputs.

The Figure 3 Represents The Architecture Of 16-Bit Brent Kung Adder Which Consumes Less Area When Compared To Other Parallel Prefix Adders, The Computation Involves Three Processes They Are

- Preprocessing Stage
- Carry Look Ahead Operation In Parallel Prefix Form

- Post Processing Stage

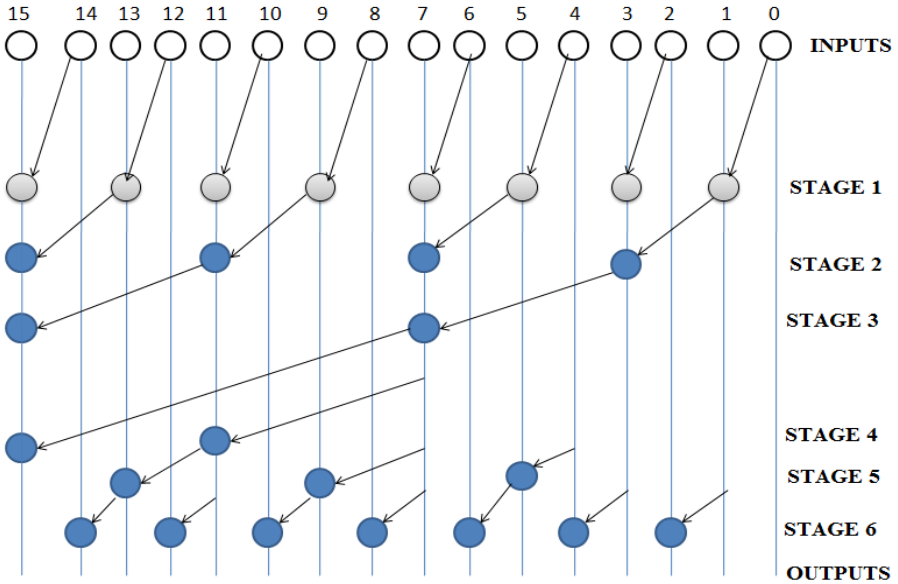

Figure 3: Architecture Of 16-Bit Brent Kung Adder

In The Pre Processing Stage, The Generate And The Propagate Signals Are Computed For The N-Bit Input Values Given To The Adder. Half Adders Are Mainly Used To Compute The Generate And Propagate Signals In This Stage.

The Next Stage Of The Brent Kung Adder Is Known As Carry Look Ahead Stage Because It Generates The Carry Signal At Different Stages By Performing The Carry Look Ahead Operation, The Two Binary Tree Structure Are Involved To Compute The Carry Signals, They Are Named As

- Forward Tree Structure
- Reverse Tree Structure

The Forward Binary Tree Will Compute The Carry Signals Generated By The Bits 0, 1, 3, 7. The Reverse Binary Tree Will Compute The Remaining Carry Signals. These Two Tree Structures Compute The Carry Signal At The Same Time So That The Delay Can Be Reduced When Compared To Other Conventional Adders.

The Final Stage In This Architecture Is The Sum Generation Stage. This Stage Is Also Known As Post Processing Stage Where Each Sum Bits Are Added In The Parallel Form And They Are Summed Up Together By Using Xor Gate.

The Addition Of $C \times Dr + D \times Cr$ Is Performed Using Brent Kung Adder. The Kogge Stone Adder Is Used In The Previous System For The Addition Operation, But This Covers Large Area For High Order Bits So The Power Consumption Will Be High In Order To Overcome This Problem Brent Kung Adder Is Used Which Has The Less Area When Compared To Kogge Stone Adder For Higher Order Bits. Hence This Logarithmic Structure Is Beneficial For The System Or Application Where Reduction Of Area Is Highly Concerned And It Reduces The Expenses Of Area And The Complexity Of The Structure.

VIII. Subtractor And Sign Set Block Operation

The Sum Value From The Brent Kung Adder Is Subtracted From The Cr×Dr As Per The Equation 1.The Values Are Converted Into Integer Before Performing The Subtraction Operation For Easy Computation Of Output. Finally The Msb Bit In The Sign Set Is Considered And The Final Output Value Is Obtained With The Sign. The Final Obtained Result Will Be Approximately Equal To The Product Value Of The Precise Multiplier. This Approximate Computation Is Used In The Application Where Exactness Of The Operation Is Not That Much Important For Example In Image Processing Method, Exactness Of The Obtained Value Is Not Given That Much Important In Such Cases This Approximate Multiplication Can Be Used.

IX. Results And Discussions

The Following Simulation Tools Are Used To View The Results For The Approximate Multiplication Process

- Xilinx Ise Simulator
- Modelsim

The Simulation Result In The Figure 4 Explains The Output Obtained For Unsigned Whole Numbers. Here The Inputs Are Given As 2 And 5 And Final Multiplied Output Will Be 10 Which Are Indicated As Out1 In The Binary Form. Initially The Numbers Are Converted Into Binary (Here It Is Represented As 5 Bit Binary Number). In The Fig 4, A And B Represents The Inputs 2 And 5 Which Is Represented In 5 Bit Binary Format. The Msb Bit Of The Two Inputs Is Used To Determine The Sign Of The Output Value With The Help Of The Sign Detector. The Rounded Off Values Will Be Obtained As 2 And 5 Since It Is Given As Whole Numbers There Is No Need For Rounding Operation. As Specified In The Equation 1.These Values Are Multiplied Using Barrel Shifter In The Previous System Which Has Some Delay. The Multiplied Values Are Added Using Kogge Stone Adder In The Previous System. Finally The Output Is Obtained As 10 Bit Binary Number (Out1).The Msb Bit Of The Out1 Represents The Sign Of The Output Which Is Determined Using The Sign Set. If The Obtained Msb Bit Is '0' Then The Sign Is Positive, If It Is '1' Then The Sign Is Considered As Negative. Since The Obtained Output Value Is In Positive In Fig 4, The Msb Bit Is Represented As '0', The Remaining Bits Of The Out1 Represents The Output Value.

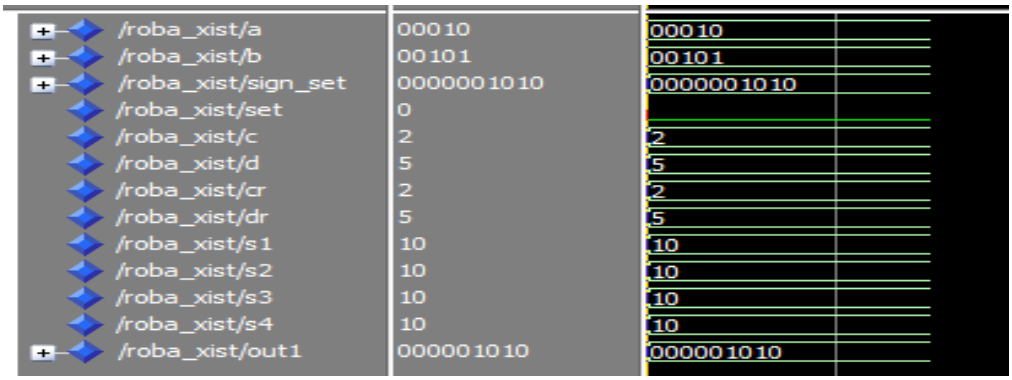

Figure 4: Multiplication Of Non Floating Numbers

For Floating Point Number Multiplication Consider The Input As C= 2.2 And D=2.2 As Two Inputs .Initially These Values Are Converted Into 8 Bit Binary Number For Sign Detection Then The Msb Bits Are Extracted And By Applying The Xor Operation The Sign Of The Final Output Value Is Obtained And It Is Forwarded To The Sign Set, The Fig 1 Will Clearly Shows The Forwarding Of Sign Bit From Detector To The Sign Set. Let The Rounded Off Values For The Inputs C And D Obtained After The Rounding Off Block Are Cr=2 And Dr=2 Respectively.

As Per The Equation 1 The Approximate Multiplication Of Two Floating Point Numbers Is Performed By Three Multiplication, One Addition And One Subtraction Operation. The Three Multiplication Operations I.E $C\times Dr$, $D\times Cr$, $Cr\times Dr$ Are Performed Using Booth Signed Multiplier. Here The Multiplication Is Carried Out As 2×2.2 $(C\times Dr)$, 2.2×2 $(D\times Cr)$, $2\times2(Cr\times Dr)$.

These Will Be In The Form Of 8 Bit Binary Number, So That It Is Convenient For The Booth Sign Multiplier To Perform The Multiplication Operation. The Simulation Result In Fig 5 Shows The Value Of Intermediate Output Cr×D [I.E $2\times2.2= 4$] Which Is Performed Using Booth Sign Multiplier As An Example .Similarly The Values For C×Dr, Cr×Dr Is Obtained. Since The Booth Sign Multiplier Has The Lowest Delay Than Any Other Multipliers As Referred In The Paper It Is Used In The Proposed System For Multiplication Purpose To Reduce The Delay. The Value A And B In The Fig 5 Represents The Binary Form Of The Values 2.2 And 2. The Final Represents The Corresponding Output Value I.E 4.4($2.2\times2=4.4$) As 16 Bit Binary Number. Similarly The Values For C×Dr, Cr×Dr Is Obtained.

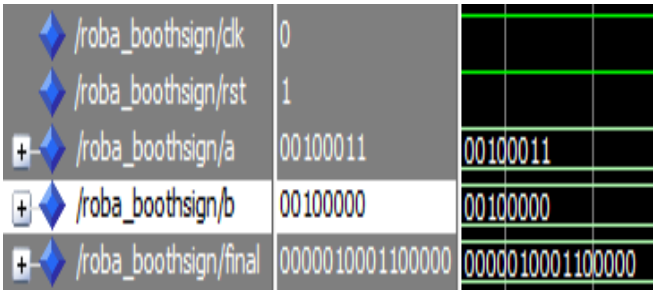

Figure 5: Simulation Result Of Booth Signed Multiplier

The Addition Of $C \times Dr + D \times Cr$ Is Performed Using Brent Kung Adder . The Simulation Result In Fig 6 Shows The Result Of The Addition Process. As The Input Values Are Considered As 2.2 And 2.2 , The Intermediate Results Obtained From Booth Signed Multiplier Will Be 4.4[$C \times Dr$], 4[$Cr \times Dr$] And 4.4[$Cr \times D$] Respectively In The Form Of 16 Bit Binary Number .In The Simulation Result The Value Of X And Y Represents The Value Of 4.4 And 4.4 Respectively . Then The Output Value [4.4 + 4.4 = 8.8] Is Obtained Using Brent Kung Adder Is Represented As Sum In The Figure 6.

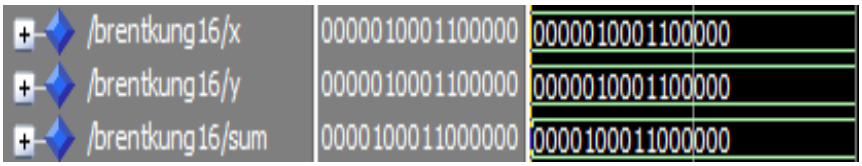

Figure 6: Simulation Result Of Brent Kung Adder

This Sum Value From The Brent Kung Adder Is Subtracted From The $Cr \times Dr$ As Per The Equation 3.7.The Values Are Converted Into Integer Before Performing The Subtraction Operation For Easy Computation Of Output. Finally The Msb Bit In The Sign Set Is Considered And The Final Output Value Is Obtained With The Sign. The Final Simulation Result Is Shown In Fig 7, By The Approximate Computation The Final Product Value Obtained For Multiplication Of Two Floating Point Numbers (2.2 And 2.2) Is Represented In The Form Of Fraction(.80) And Real Part (4) , Which Is Equal To 4.80.This Output Value Is Approximately Equal To The Original Product Value 4.84 Obtained By Multiplying 2.2 And 2.2 .

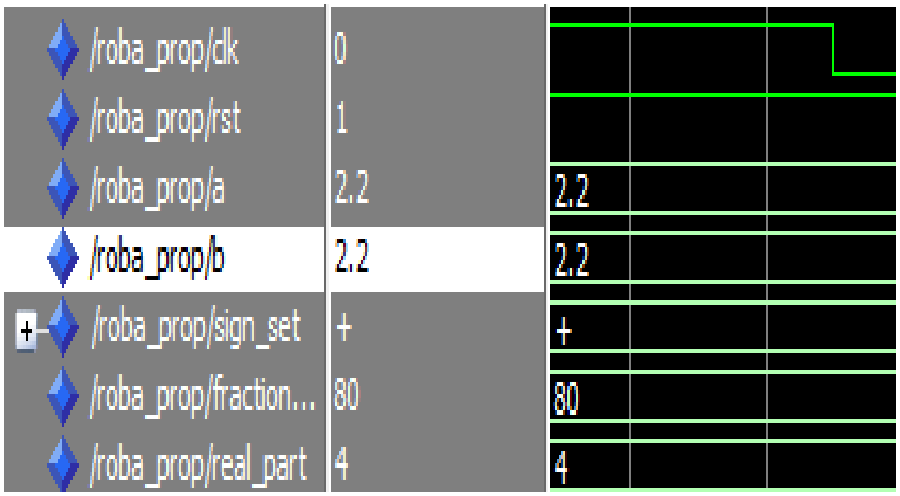

Figure 7: Simulation Result Of Proposed Approximate Multiplier Based On Rounding.

The Below Table I, Shows The Number Of The Components , Lut's And Slices, Bounded Iob's Used In The Proposed Architecture. It Is Clear That The Proposed System Uses Less Area Than The Previous System. This Increases The Speed And Reduces The Power Consumption Which Is The Major Requirement In The Processor Applications.

Table I: Device Utilization Summary

Slice Logic Utilization	**Used**
Number Of Slice Registers	16
Number Used As Flip Flops	16
Number Of Slice Luts	310
Number Used As Logic	310
Number Of Occupied Slices	102
Nummber Of Muxcys Used	192
Number Of Lut Flip Flop Pairs Used	310
Number With An Unused Flip Flop	298
Number Of Fully Used Lut-Ff Pairs	12

Number Of Unique Control Sets	1
Number Of Bonded Iobs	37
Number Of Bufg/Bufgmuxs	1
Number Used As Bufgs	1
Number Used As Bufgmux	0

No. Of Occupies Slices=Power, Bonded Iob's=Area, Fanout=Time

The Power And Delay Bar Graph Represented In Figure 8 Shows That The Proposed System Has Consumed Less Power And Delay When Compared To Previous System. This Paper Thus Proposes An Approximate Multiplier Achieves The Reduction Of Area, Power Consumption And Delay Which Is The Major Design Requirements In The Digital Processing Systems.

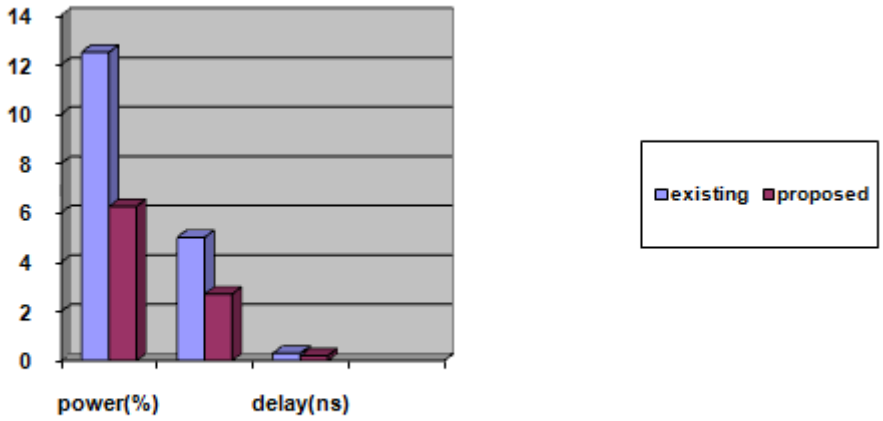

Figure 8: Power And Delay Bar Graph

X. Conclusion

The Approximate Multiplier Which Is Based On Rounding Is Designed Using Booth Signed Multiplier And Brent Kung Adder Which Is More Efficient Than The Previous Approximate And Accurate Multipliers. This Is Applicable Where The Area Is Mostly Concerned Than The Delay, Since Brent Kung Adder Uses Less Area Than Other Parallel Prefix Adders It Consumes Less Area Leads To Reduced Power Consumption. The Efficiency Of The Proposed Approximate Multipliers Were Evaluated By Comparing With Some Of Previous Approximate Multipliers And The Results Reveals That Proposed Approximate Multiplier Is Efficient In The Applications Where The Area Of The System Is Highly Concerned.

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