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Performance Analysis of VLSI Circuits In 45nm Technology

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Abstract : *The optimization of power consumed in digital blocks of an Integrated Circuit while preserving the functionality is performed by Electronic Design Automation (EDA) tools. There is a significant increase in the power consumption of Very Large Scale Integration (VLSI) chips due to the increasing speed and complexity of today's designs. Reduction of power is a great challenge. With today's world of advancement in the IC technology there are over 100 million transistors, clocked at over 1 GHz which means manual power optimization would be very slow and a great certainty of errors, hence Cadence tools are necessary. Performance improved for 10T Full Adder,14T Full Adder and 28T Full Adder Circuit in terms of power and area reduced in 45nm technology Cadence SPECTRE simulator.*

Keywords *- 10T Full adder, 14T Full adder, 28T Full adder, low power, low area and VLSI.*

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I. Introduction

With every generation of VLSI technology scaling, the researchers are improving the performance of computer systems. Unfortunately, they consume a lot of power; in fact their power densities and accompanying heat generation are rapidly approaching levels that are comparable to nuclear reactors . These high power densities reduce chip reliability and life expectancy, increase cooling costs and even cause environmental issues for large data centers. At the other end of the performance spectrum, power issues pose problems for smaller mobile devices with limited battery capacities. In these devices, the use of larger memories and faster processors further reduce the battery life. Hence, improvements in microprocessor technology will reach a standstill, if cost effective solutions to power problems are not provided. Power management is a integrative field that involves many conditions like temperature, energy, high speed work stations and reliability, each of which is complex.

This paper provides a survey of various power reduction techniques that are used to reduce the total power consumed by a microprocessor system at circuit level. Full adders have been use as a digital circuit in various estimation circuits to carry out arithmetic operations like addition, subtraction, multiplication, address calculation and MAC unit etc. Apart from arithmetic operations, adders are utilized to generate memory locations in different architectures of microprocessors and cache memories. Thus improvement in the full adder would prove more beneficial for all the circuits where its application has a significant effect in the performance of the circuit where it has been employed. The most important parameters to be kept in consideration are compactness and power which affects the performance and usefulness of any VLSI circuit. The system specifications are processor Intel (R) core (TM) i5-4570 CPU@3.20GHz.,3.20GHz.Installed memory (RAM) 4 GB (usable memory is 3.43GB) and system type: 32-bit operating system (OS). This paper is formed as follows Section II presents the literature review on 10Tfull adder, 14Tfull adder and 28Tfull adder Section III presents the methodology for 10Tfull adder, 14Tfull adder and 28Tfull adder and also discussed the low power analysis, High speed and low area. Section IV shows the simulation results and they are discussed clearly, finally the paper is concluded with Section V.

II. Literature Review

Adders are basic building block of estimation Very-large-scale integration (VLSI) circuits found in processor and microcontroller inner Arithmetic and Logic units. Upgrading the performance of the adder thus becomes imperative which would certainly result in the improvement of digital electronic circuits where adder is employed [1]. In this digital world due to increase in demand of portal electronic components low power design of VLSI playing major role. Power consumption in a circuit is mainly static power and dynamic power [2]. Full adders have been use as a base circuit in various estimation circuits to carry out arithmetic operations like addition, subtraction [3].

Apart from arithmetic operations, adders are utilized to generate memory locations in different architectures of microprocessors and cache memories. Thus improvement in the full adder would prove more beneficial for all the circuits where its application has a significant effect in the performance of the circuit in which it has been employed. The most important parameters to be kept in consideration are compactness and power which affects the performance and usefulness of any VLSI circuit [4-5].

III. Design Methodology

1. 14T FULL ADDER

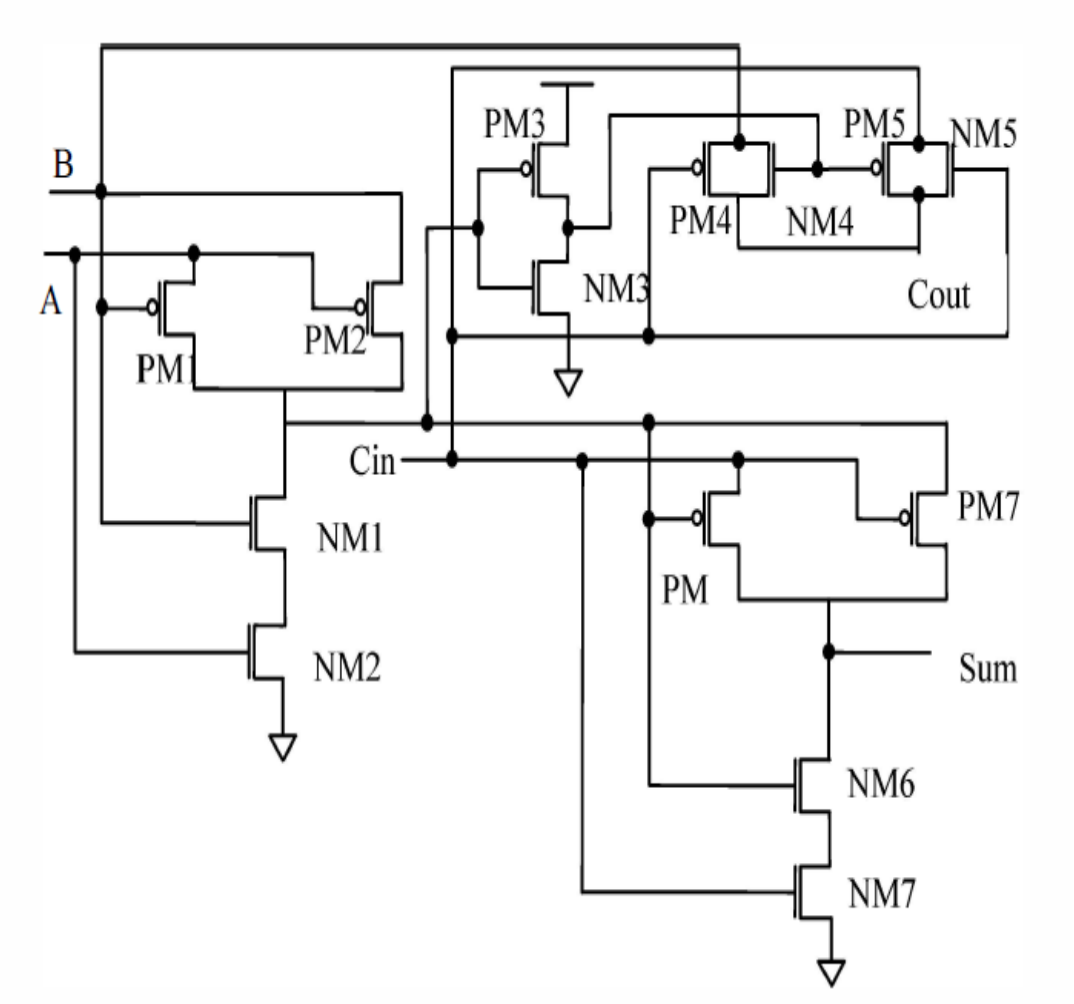

Figure 1: 14T Full Adder

Need of Reduction in number of transistors in the conventional full adders, led to the application of pass transistor based XOR and XNOR circuits which resulted in the development of 14T full adder [11] as shown in figure l. Application of 14T full adder ensured improved delay performance and reduced power consumption over previous works in the full adders. The adder was also employed to work well with high performance multipliers with reduced power consumption. However the adder did not showed improvement in threshold power loss. More over the 14T adder consumed significant power which is yet to be reduced much lower level. The power waveform of 14T full adder signifies the power consumed by the circuit over the period of simulation, obtained using Cadence SPECTRE simulator. The average power [9] [10] over this simulation has been indicated on the waveform which needs to be improved. The leakage current contributes the amount of leakage power in the CMOS circuit. More is the leakage current more will be the leakage power which must be lowered in order to make the circuit more power efficient. The amount of leakage current here is result of integration of leakages due to individual transistors. Hence it may be concluded that if number of transistors is reduced the leakage would be less. Further, as described in equation 1, it may be noted that on reducing the supply voltage, which results in reduction of leakage current as well, would reduce the power consumption to a significant level.

2. 10T FULL ADDER

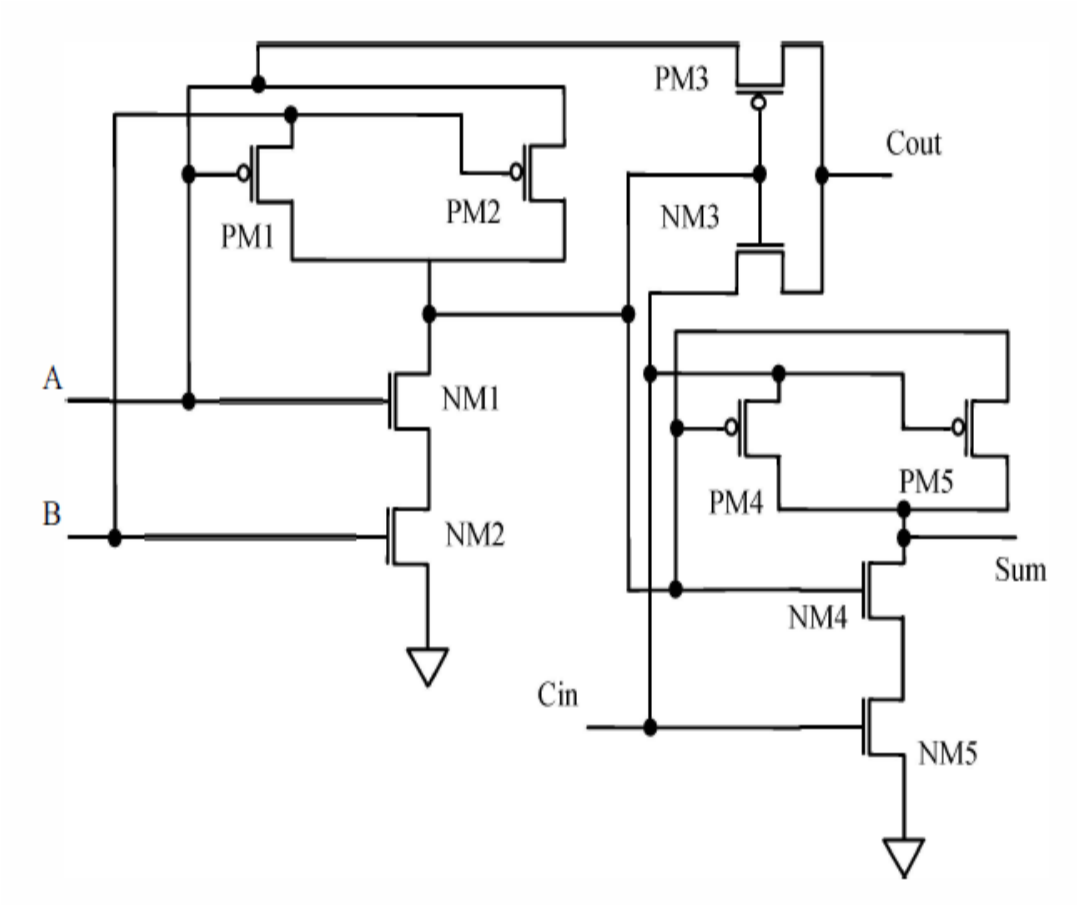

Figure 2: 10T Full Adder

Full adder presented in this paper employs 10 MOSFETs as shown in figure 5. In comparison the 10T full adder Fig [1] showing better performance than earlier full adders that use more number of transistors. The Boolean expressions showing the full adder operation are defined below:

$$SUM = A \oplus B \oplus C \text{.....(1)}$$

$$COUT = AB + BC + AC \text{.....(2)}$$

The full adder shown here has been analyzed for different parameters later in this paper. The l0T full adder presented in this paper, shows optimized results in power and area.

This paper provides a survey of various power reduction techniques that are used to reduce the total power consumed by a microprocessor system at circuit level. Full adders have been use as a Conventional circuit in various arithmetic circuits to carry out arithmetic operations like addition, subtraction, multiplication, address calculation and MAC unit etc. Apart from arithmetic operations, adders are utilized to generate memory locations in different architectures of microprocessors and cache memories. Thus improvement in the full adder would prove more beneficial for all the circuits where its application has a significant effect in the performance of the circuit where it has been employed. The most important parameters to be kept in consideration are compactness and power which affects the performance and usefulness of any VLSI circuit.

3. 28T Conventional Full Adder Circuit

The 1-bit full adder cell has 28 transistors. For complex gates with large fan-ins the CMOS design style is not area efficient technique. Thus, care must be taken when a static logic style is selected to realize a logic function. The pseudo NMOS technique is straight forward. A classical design of stand of normal static complementary metal-oxide semiconductor (CMOS) full adder is based on regular CMOS structure with conventional pull-up and pull-down transistor providing full -swing output and good driving capabilities.

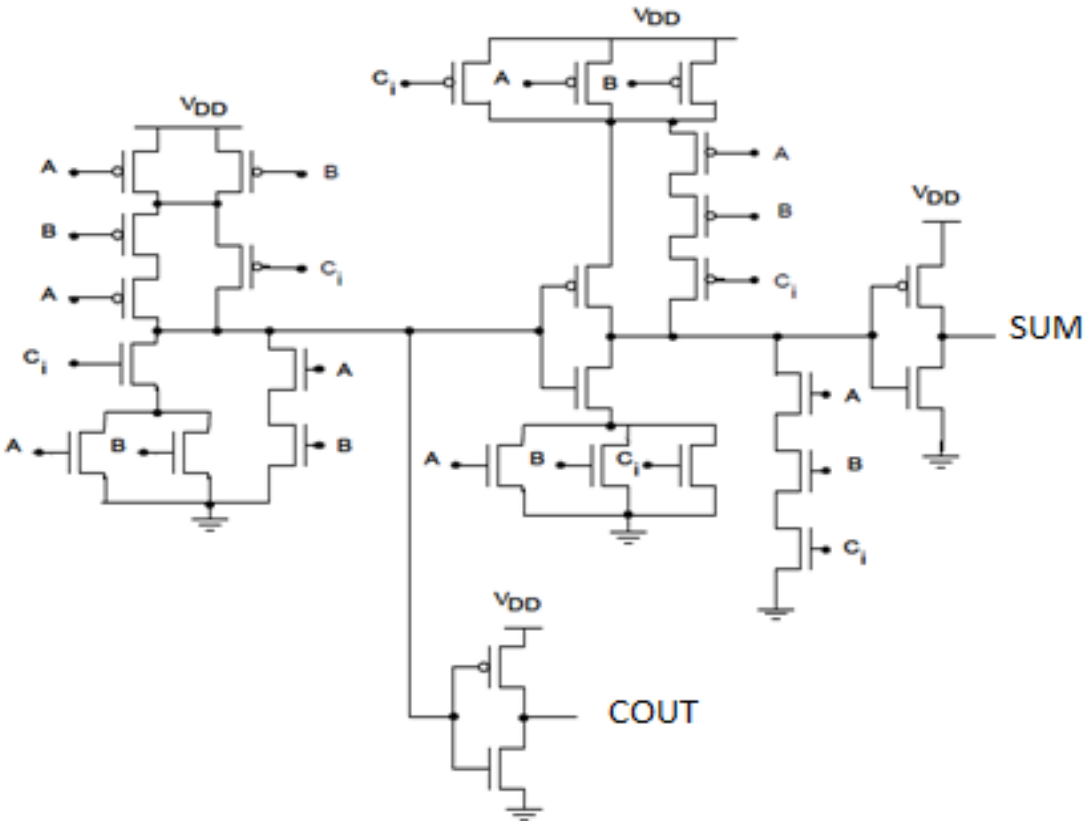

Figure 3: 28T Full Adder Circuit.

The full adder consists of three inputs A, B, and C_{in} one bit each it calculates the two outputs Sum and carry both of them are one bit each this is the operation of the full adder.

IV. Synthesis And Simulation Results

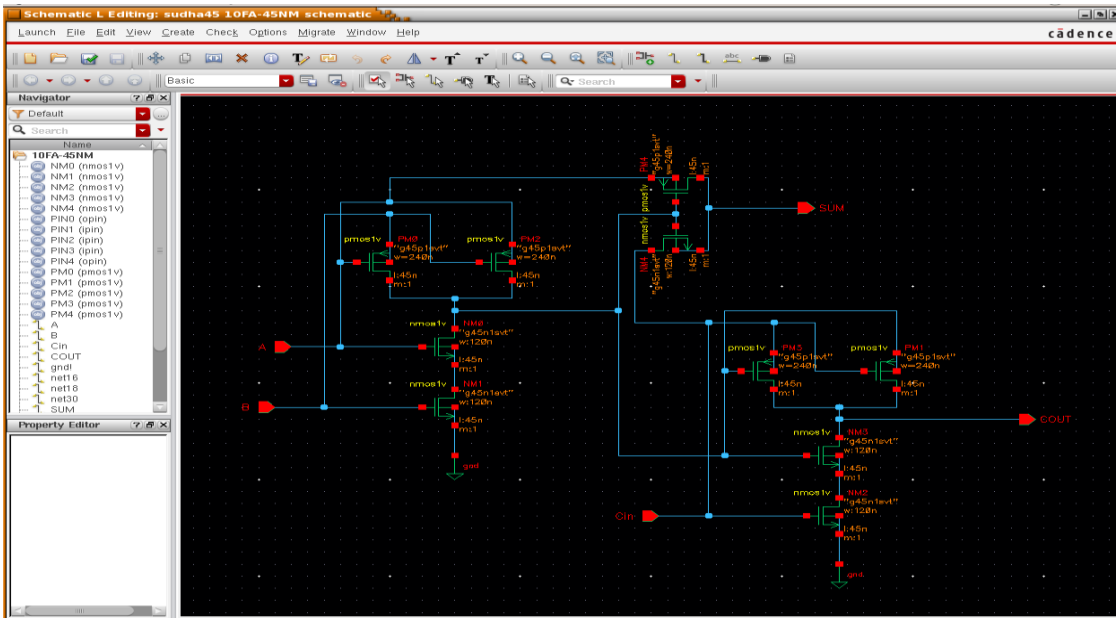

Figure 4: 10T Full Adder Schematic diagram

It is observed from the Figure 4, The PMOS and NMOS transistors schematic diagram consist of width are 240nm and 120nm at supply voltage 1 V. Both rise time and fall time (100f)sec and the simulation of the proposed 10T Full Adder schematic diagram was carried out using 45nm technology.

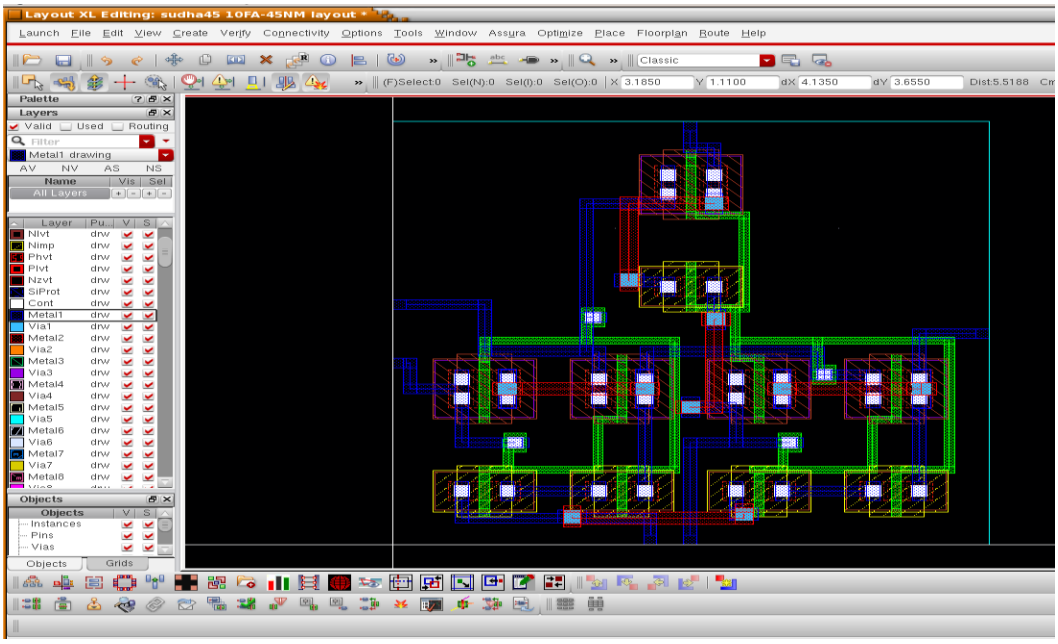

Figure 5: 10T Full Adder Layout diagram in 45nm technology

It is observed from the Figure 5, 10T Full Adder Layout diagram is combination of PMOS and NMOS transistors consist of width are 240nm and 120nm ,Green color is poly silicon and blue color is Metal1,where A, B, Cin, Sum, Cout, V_{dd} and ground are connected to Metal1, 10T Full Adder Layout diagram at 1 Volts in 45nm Technology.

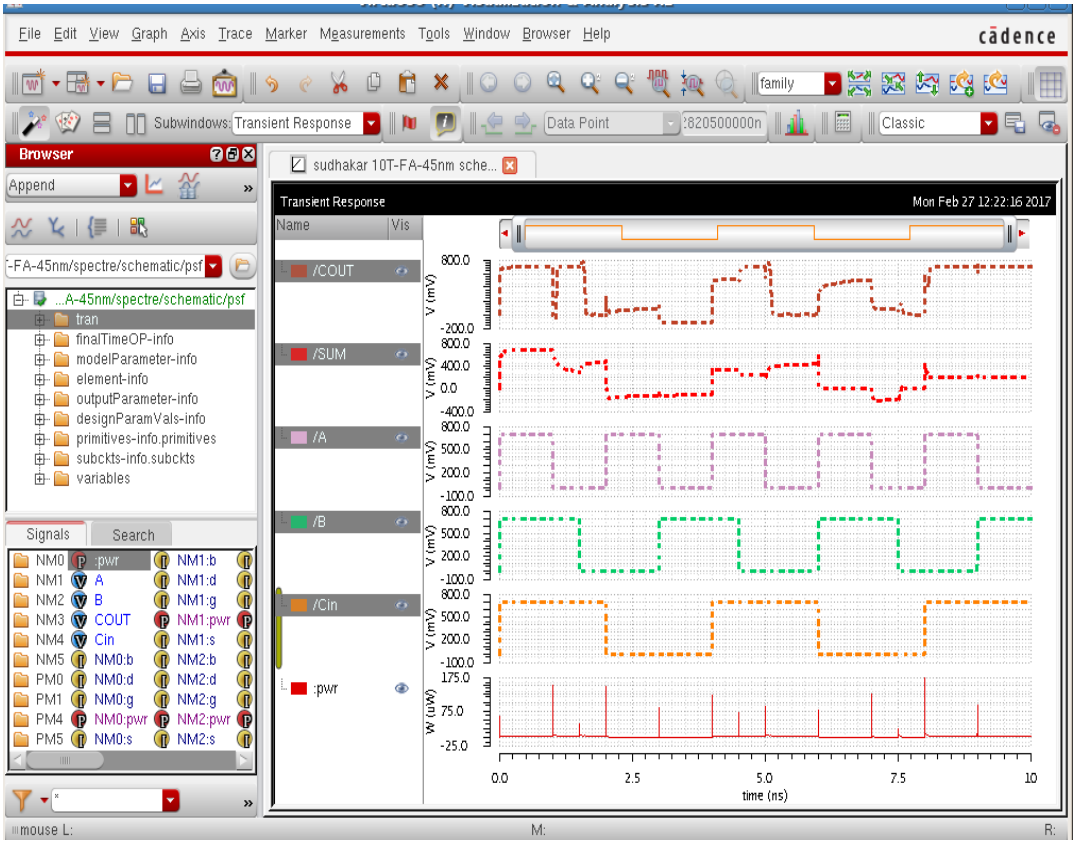

Figure 6: 10T Full Adder Output waveform.

From shown in figure 6 10T Full Adder simulation result of output waveform at 1Volts in 45nm technology.

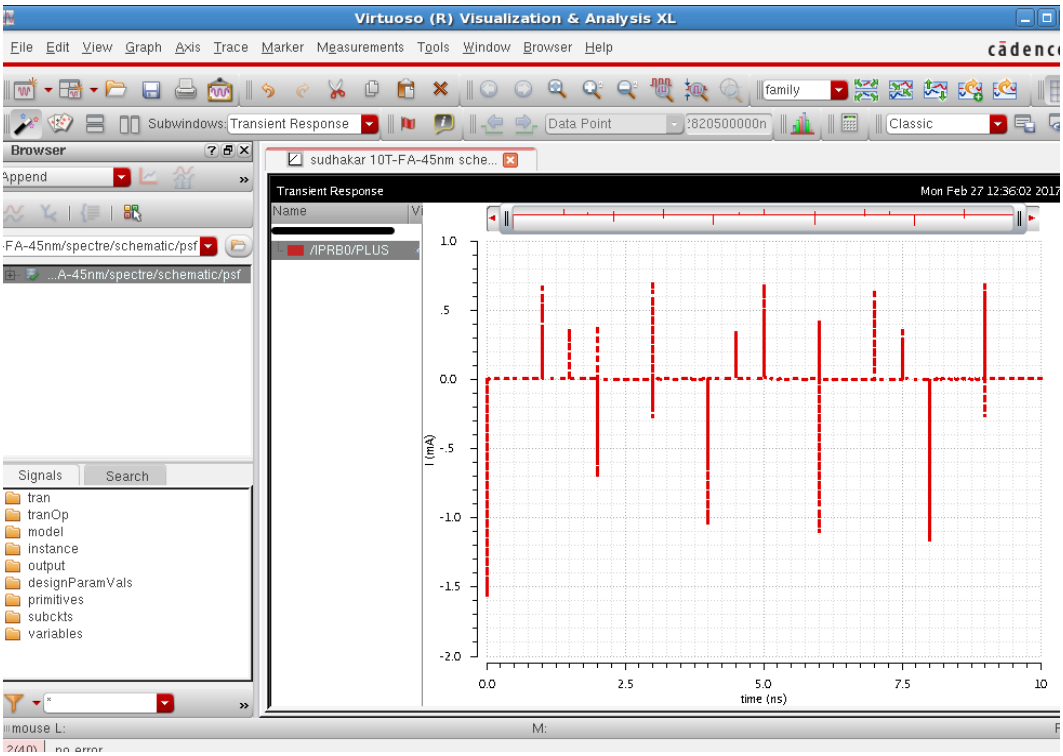

Figure 7: Leakage current waveform of 10T full adder in 45nm technology

As shown in figure 7, 10T Full Adder simulation result of Leakage current waveform at 1Volts in 45nm technology

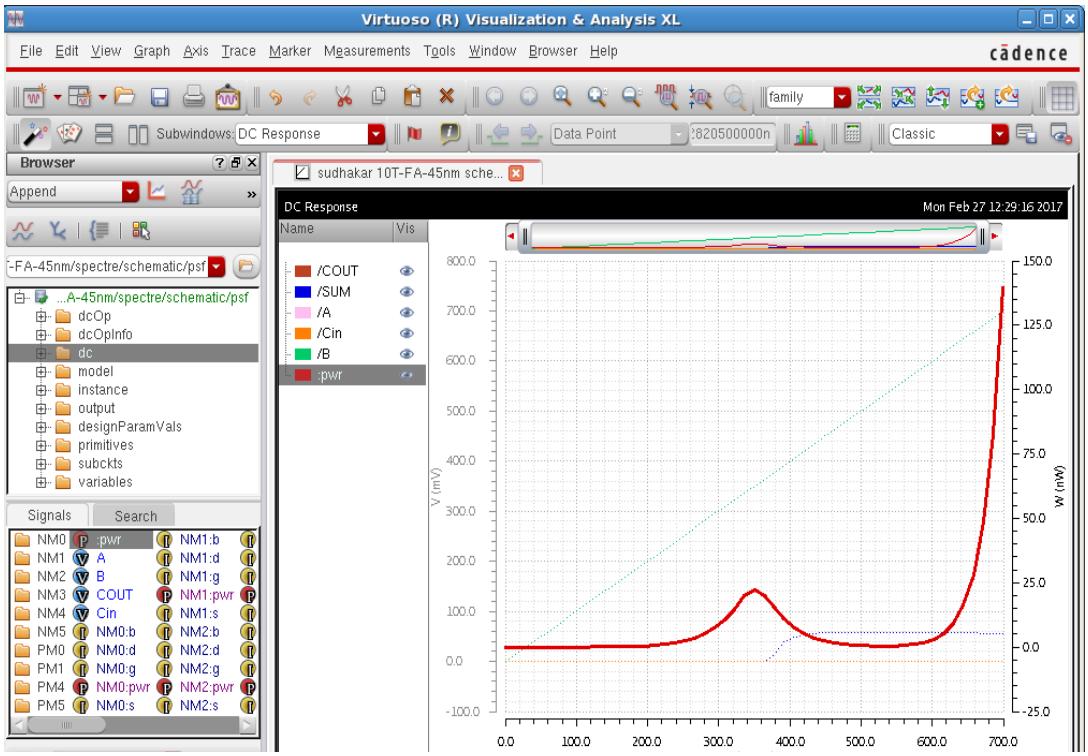

Figure 8: 10T full adder Power waveform

From shown in Figure 8, 10T Full Adder simulation result of DC power waveform at 1Volts in 45nm technology.

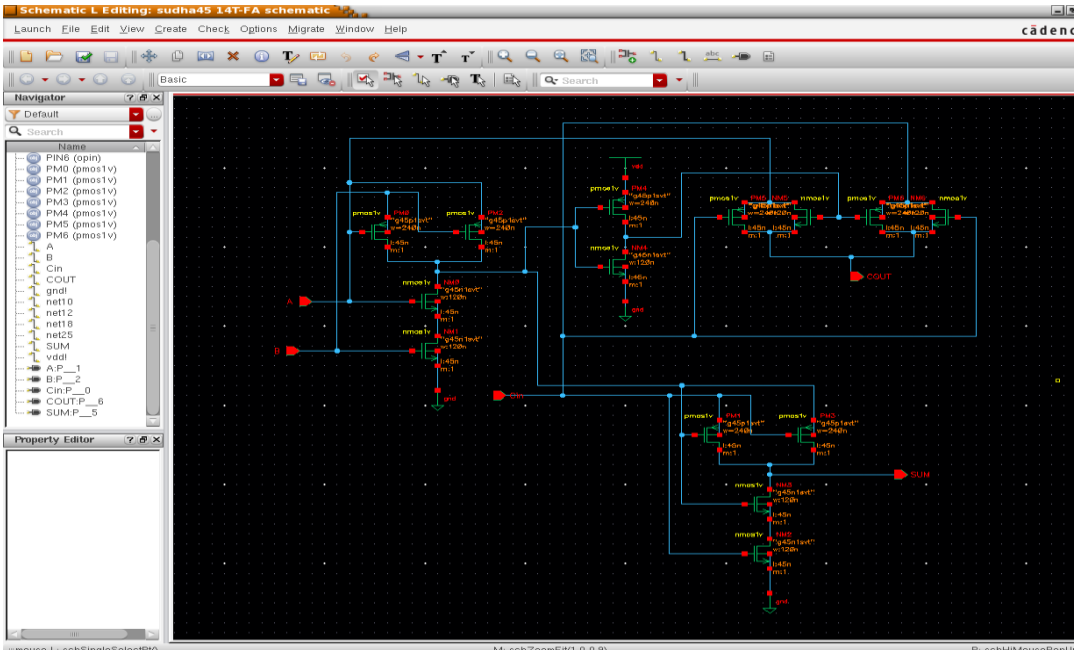

Figure 9 14T Full Adder Schematic in 45nm Technology

It is observed from the Figure 9, The PMOS and NMOS transistors schematic diagram consist of width are 240nm and 120nm at supply voltage 1 V. Both rise time and fall time (100f)sec and the simulation of the proposed 14T Full Adder schematic diagram was carried out using 45nm technology.

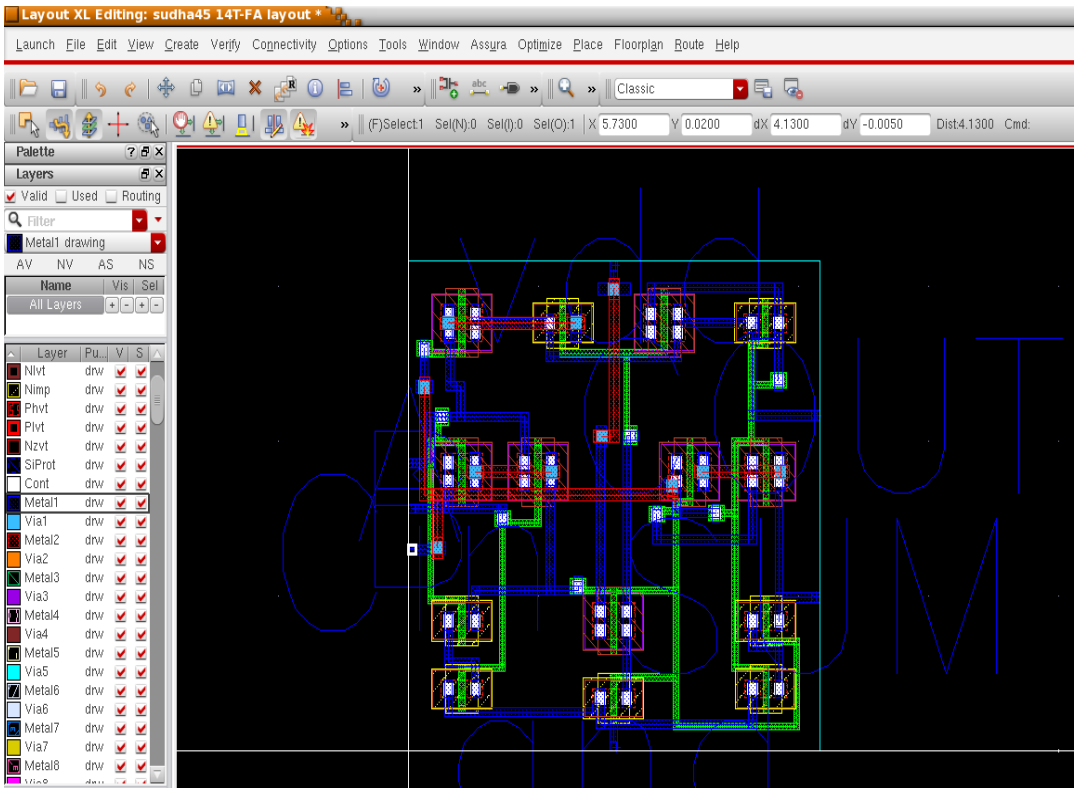

Figure 10 14T Full Adder Layout diagram in 45nm Technology

It is observed from the Figure 10 14T Full Adder Layout diagram is combination of PMOS and NMOS transistors consist of width are 240nm and 120nm ,Green color is poly silicon and blue color is Metal1,where A, B, Cin, Sum, Cout, V_{dd} and ground are connected to Metal1, 14T Full Adder Layout diagram at 1 Volts in 45nm Technology.

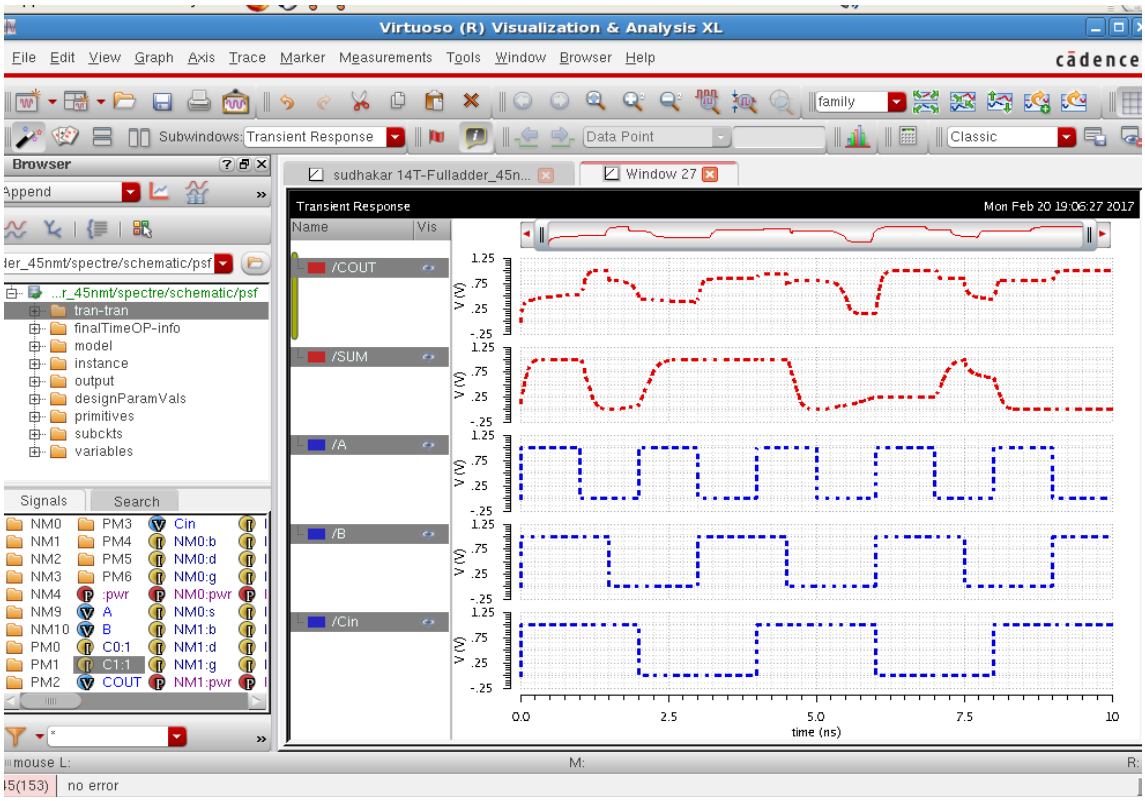

Figure 11 14T Full Adder output waveform

As shown in Figure 11 14T Full Adder simulation result of output waveform at the frequency 100MHz and 1Volts in 45nm technology.

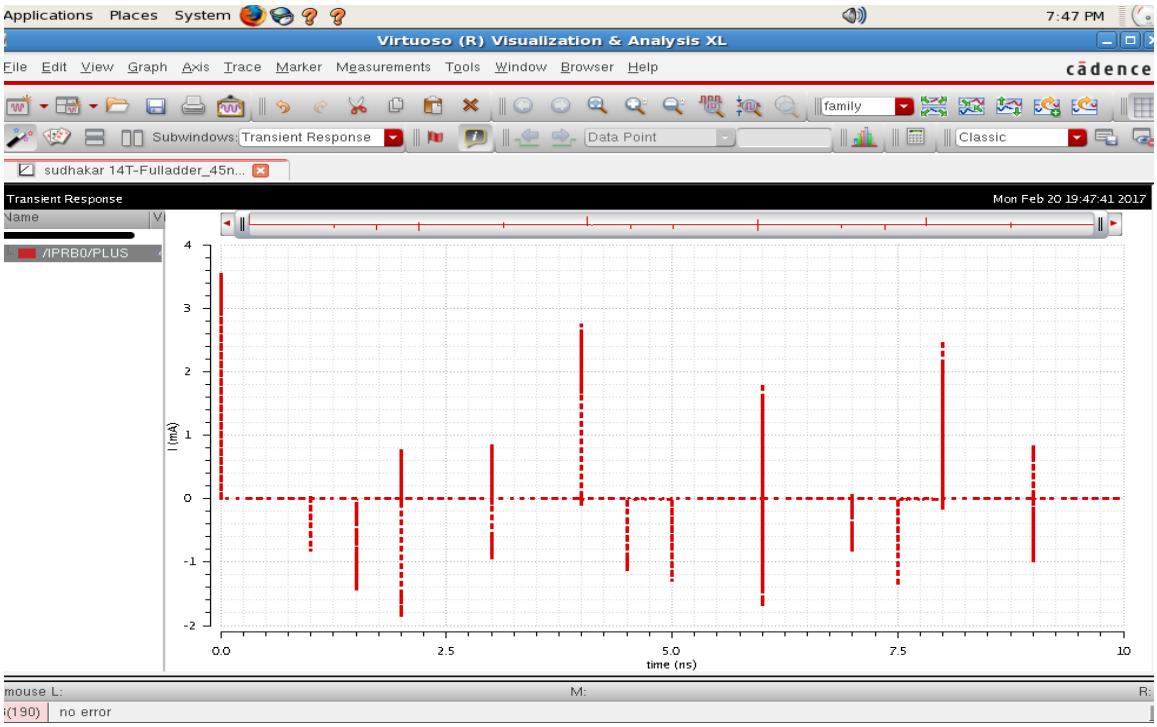

Figure 12: 14T full adder Leakage current waveform.

As shown in figure 12, 14T Full Adder simulation result of Leakage current waveform at 1Volts in 45nm technology

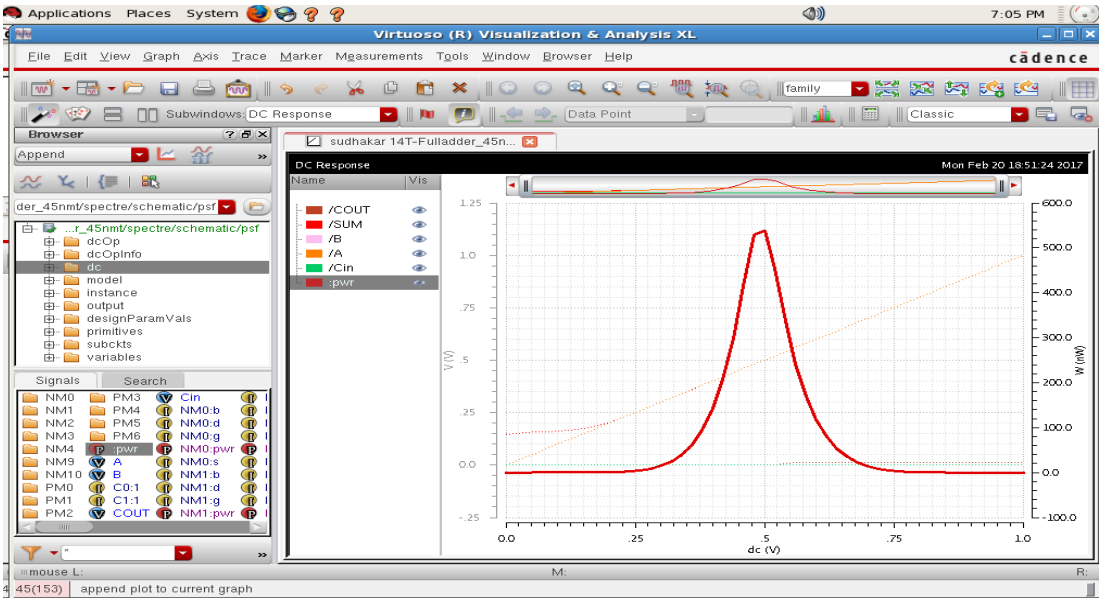

Figure 13: 14T full adder Power waveform

As shown in figure 13, 14T Full Adder simulation result of DC power waveform at 1Volts in 45nm technology.

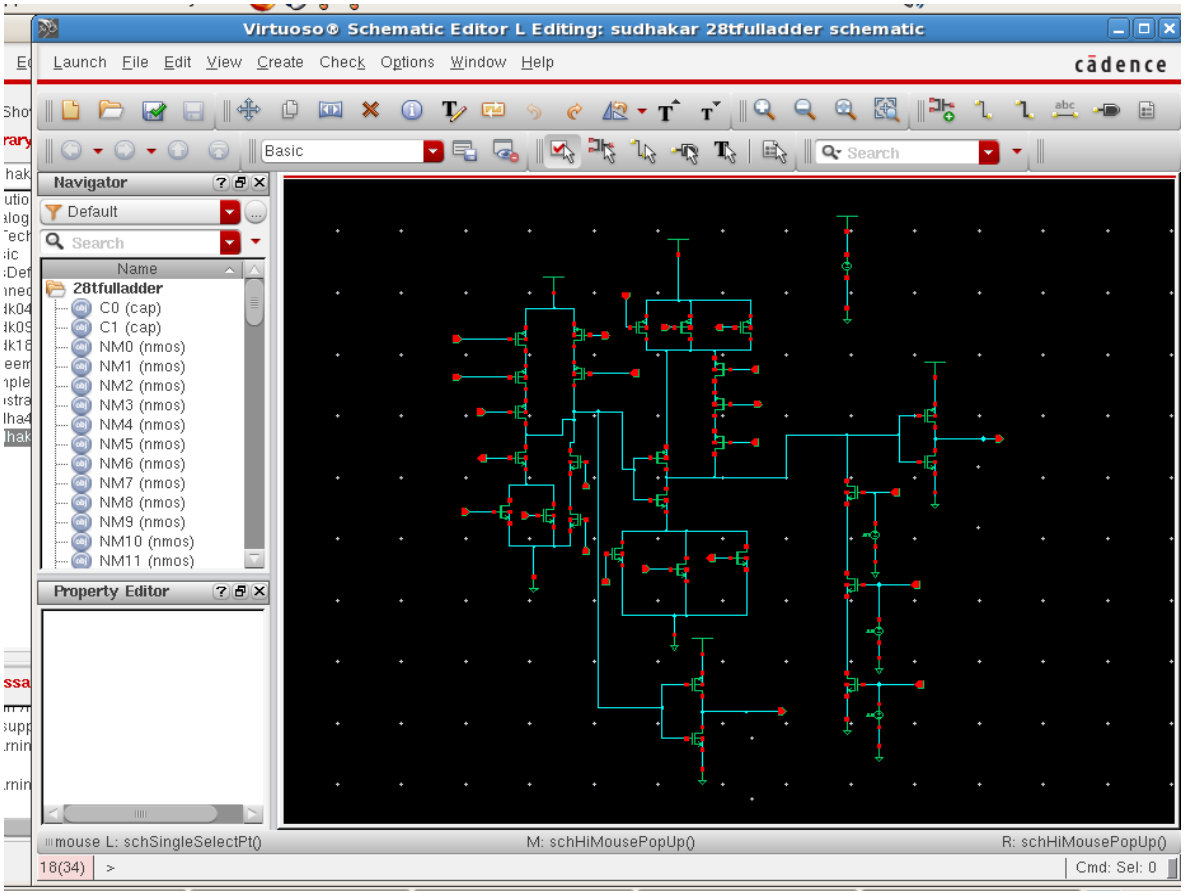

Figure 14: Schematic diagram of 28T Full Adder in 45nm technology

It is observed from the Figure 14, The PMOS and NMOS transistors schematic diagram consist of width are 240nm and 120nm, Load capacitance is 10fF, at supply voltage from [0.7-1.5] V. Both Rise time and fall time (100f)sec and the simulation of the proposed 28T Full Adder schematic diagram was carried out using 45nm technology.

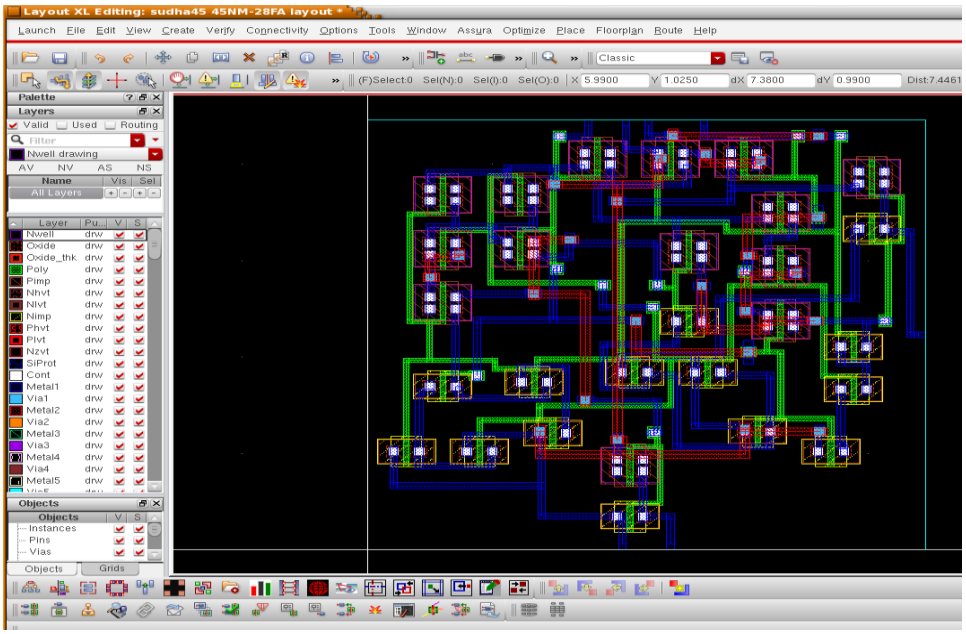

Figure 15: Layout diagram of 28T Full Adder in 45nm Technology

It is observed from the Figure 15, 28T Full Adder Layout diagram is combination of PMOS and NMOS transistors consist of width are 240nm and 120nm ,Green color is poly silicon and blue color is Metal1,where A, B, Cin, Sum, Cout, V_{dd} and ground are connected to Metal1, 28T Full Adder Layout diagram at 1 Volts in 45nm Technology.

Table 1: Specification of 28T Full Adder in 45nm technology

Specification	NMOS	PMOS
Library name	Gpdk 45	Gpdk 45
Length	45 nm	45 nm
Total width	120 nm	240 nm
Finger width	120nm	240 nm
Rise/fall time	100f s/100f s	

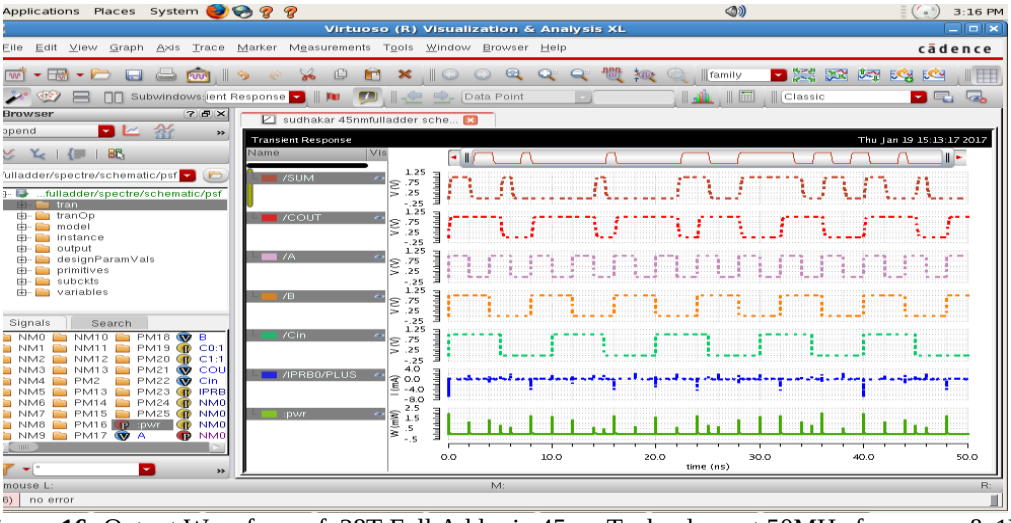

Figure 16: Output Waveform of 28T Full Adder in 45nm Technology at 50MHz frequency & 1V

It is observed from the Figure 16, The PMOS and NMOS transistors simulation result of output waveform consist of width are 240nm and 120nm, Load capacitance is 10fF, at supply voltage 1 V. Both Rise time and fall time (100f) in 45nm technology.

Table 2: Comparison of power and area 10T Full adder, 14T Full adder and 28T full adder in 45nm Technology

Parameter	Power(nW)
14T Full adder [1]	78.21
Proposed of 14T Full adder	29.67
% of 14T Full adder Power Reduced	62.06%
% of 14T Full Area Reduced [nm^2]	37.93%
10TFull adder [1]	21.04
Proposed of 10T Full adder	8.561
% of 10T Full adder Power Reduced	59.31%
% of 10T Full Area Reduced [nm^2]	40.68%
28T Full adder [2]	351.1
Proposed of 28T Full adder	205.4
% of 28T Full adder Power Reduced	41.49%
% of 28T Full Area Reduced [nm^2]	58.50%

It is observed that the table 2, power is reduced by 59.31%% for 10T Full Adder , 62.06% for 14T Full Adder and 41.49% for 28T Full Adder. area is reduced by 40.68 % for 10T Full Adder , 37.93% for 14T Full Adder and 58.50% for 28T Full Adder**.** The proposed results are compared with the previous existing designs in terms of power and area. It is observed that the figure 17 , power is reduced by 59.31%% for 10T Full Adder , 62.06% for 14T Full Adder and 41.49% for 28T Full Adder. The proposed results are compared with the previous existing designs in terms of power and area.

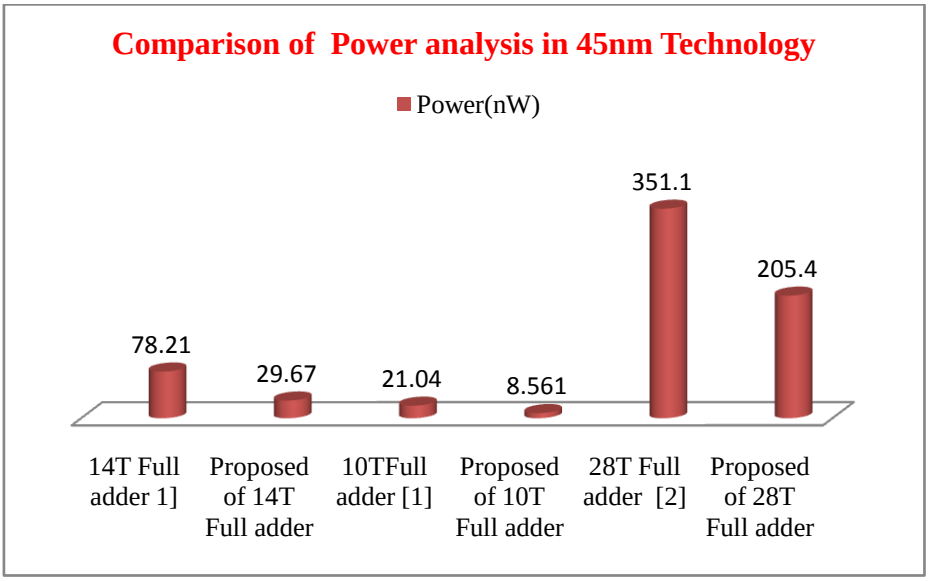

Figure 17: Comparison of Power analysis in 45nm technology.

V. Conclusion

It is observed that the table 2, power is reduced by 59.31%% for 10T Full Adder, 62.06% for 14T Full Adder and 41.49% for 28T Full Adder, Area is reduced by 40.68 % for 10T Full Adder, 37.93% for 14T Full Adder and 58.50% for 28T Full Adder. The proposed results are compared with the previous existing designs in terms of power and area in 45nm technology Cadence SPECTRE simulator.

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