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Integration of Boolean Operators on Reversible Circuits Using NM-Library

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Abstract: *The study of reversible logic synthesis problem using group theory is getting more attention. By reducing the reversible circuit synthesis problem to permutation group. This permits Schreier-Sims Algorithm for the strong generating set-finding problem to be used to construct NM-based reversible circuits. This paper will present methods to integrate any three Boolean operators, as long as the integration maintains reversibility, as NM-based reversible circuit with zero-garbage output. It is shown that the order of the Boolean operator in the output vector affects the efficiency of the quantum circuit.*
Keywords: *Reversible Circuit, Quantum Cost, Quantum Circuit, Boolean Operators, Group Theory*

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I. Introduction

Reversible logic [1,2] is an interest area of research. Classical Boolean gates are mainly irreversible and cannot be used directly in the reversible circuits' synthesis [3]. Synthesis of multipurpose reversible logic gates has been proposed [4]. Reversible circuits are a fundamental requirement in the emerging field of quantum computation [5]. Reversible circuits have many applications such as: building quantum computers, bioinformatics, nanotechnology based systems, DNA computing, low power *CMOS* systems and etc [5,6,7]. Tight bounds on the synthesis of 3-bit reversible circuits using NCT library has been shown in [8]. Integration of irreversible gates in reversible circuits using NCT library has been shown in [9].

Recently, the focus on studying the reversible logic synthesis problem using group theory is rising rapidly. Investigation on the universality of the basic building blocks of reversible circuits has been done [12,13]. A relation between Young subgroups and the reversible logic synthesis problem has been proposed [14]. GAP-based algorithms that synthesize reversible circuits for various types of gate with various gate costs have been proposed [9,10,11,15]. GAP-based algorithms that is used to synthesize reversible circuits for one type of gates have been proposed [16,17,18].

The aim of the paper is to use the NM^3-based reversible circuits [18] to design a reversible circuit that simulates the construction of Boolean operators such as $AND, OR, NOT, XOR, NAND$ and NOR in a single zero-garbage output. This is done by integrating any three Boolean operators, so that the integration maintains the reversibility of the circuit. All results shown in this paper have been implemented and tested using the group theory algebraic software GAP [19].

The paper is organized as follows: Sect. 2 gives a short background on the synthesis of reversible circuit problem and shows the reduction the problem to permutation group. Sect. 3 shows the experimental results of integrating irreversible Boolean operators in a single 3-bit reversible circuit. The paper ends up with a summary and conclusion in Sect. 4.

II. Background

This section will review the basic definitions of reversible circuits, quantum cost of reversible circuits and the relationship between reversible logic circuits and permutation group theory.

2.1 Basic Definitions

Definition 1: An *n*-input *n*-output Boolean function is reversible ($n \times n$ function) if it maps each input vector to a unique output vector, i.e. a one-to-one, onto function (bijection). There are $2^n!$ reversible $n \times n$ Boolean functions. For $n = 3$, there are 40320 3-in/out reversible functions.

Definition 2: A set of reversible gates that can be used to build a reversible circuit is called a gate library L.

Definition 3: A universal reversible gate library L_n is a set of reversible gates such that a cascading of gates in L_n can be used to synthesize any reversible circuit with *n*-in/out [16].

Definition 4: Let a finite set $A = \{1, 2, \ldots, 2^n\}$ and a bijection $\delta : A \rightarrow A$, then δ can be written as,

$$\begin{pmatrix} 1 & 2 & 3 & \ldots & n \\ \delta(1) & \delta(2) & \delta(3) & \ldots & \delta(2^n) \end{pmatrix} \quad (1)$$

i.e. δ is a permutation of A. Let A be an ordered set, then the top row can be eliminated and δ can be written as,

$$(\delta(1), \delta(2), \delta(3), \ldots, \delta(2^n)) \quad (2)$$

Any reversible circuit with n-in/out can be considered as a permutation δ and (2) is called the specification of this reversible circuit.

The set of all permutations on A forms a symmetric group on A under composition of mappings, denoted by S_{2^n} [20]. A permutation group G is a subgroup of the symmetric group S_{2^n} [20]. A universal reversible gate library L_n is called the generators of the group. Another important notation of a permutation is the product of disjoint cycles [20]. For example, $\begin{pmatrix} 1,2,3,4,5,6,7,8 \\ 1,2,4,3,7,6,8,5 \end{pmatrix}$ will be written as $(3,4)(5,7,8)$. The identity mapping "()" is called the unit element in a permutation group.

2.2 Reversible Circuits

The C^nNOT gate is a reversible gate that can be used to build any n-in/out reversible circuits. It is defined as shown in Fig.1.

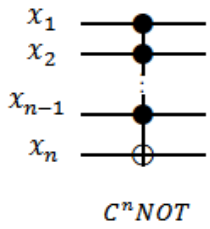

Figure 1: C^nNOT gate. The control bit line is denoted by •, and the target bit line is denoted by ⊕.

The action of C^nNOT gate is defined as follows, if the control bit lines are set to 1 then the target bit line is flipped, otherwise the target bit line is left unchanged [5]. Some special cases of the C^nNOT gate are defined as follows, C^1NOT gate with no control bit is called NOT gate. C^2NOT with one control bit is called $CNOT$ gate. C^3NOT with two control bits is called Toffoli gate. For the sake of readability C^1NOT, C^2NOT and C^3NOT will be written shortly as N, C and T respectively where the control and/or target bits will be shown in the subscript of the gate and the total number of bits will be shown in the superscript [9].

The NOT (N) gate acts on a 1-bit and it is defined as follows, it flips the input bit unconditionally. For *n*-in/out reversible circuits, there are n possible N gates. There are 3 possible N gates as shown in Fig.2.

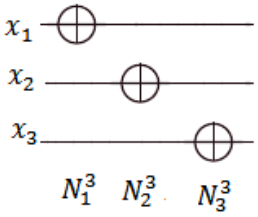

Figure 2: The 3 possible N gates for 3-bit reversible circuits.

$$\begin{aligned} \mathrm{N}_1^3&: (\mathrm{x}_1, \mathrm{x}_2, \mathrm{x}_3) \rightarrow (\mathrm{x}_1 \oplus 1, \mathrm{x}_2, \mathrm{x}_3) \equiv (1,5)(2,6)(3,7)(4,8), \\ \mathrm{N}_2^3&: (\mathrm{x}_1, \mathrm{x}_2, \mathrm{x}_3) \rightarrow (\mathrm{x}_1, \mathrm{x}_2 \oplus 1, \mathrm{x}_3) \equiv (1,3)(2,4)(5,7)(6,8), \\ \mathrm{N}_3^3&: (\mathrm{x}_1, \mathrm{x}_2, \mathrm{x}_3) \rightarrow (\mathrm{x}_1, \mathrm{x}_2, \mathrm{x}_3 \oplus 1) \equiv (1,2)(3,4)(5,6)(7,8). \end{aligned} \quad (3)$$

The Feynman (C) gate acts on two-bits and it is defined as follows, if the control bit is set to 1 then the target bit line is flipped. There are 6 possible C gates for the 3-in/out reversible circuits as shown in Fig.3.

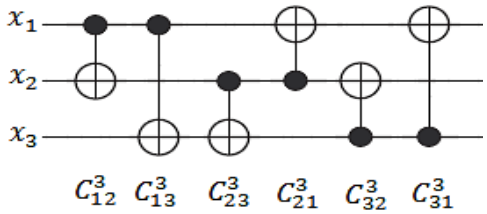

Figure 3: The 6 possible C gates for 3-bit reversible circuits.

$$\begin{aligned}
C_{12}^3&:(x_1,x_2,x_3)\to(x_1,x_2\oplus x_1,x_3)\equiv(5,7)(6,8),\\
C_{13}^3&:(x_1,x_2,x_3)\to(x_1,x_2,x_3\oplus x_1)\equiv(5,6)(7,8),\\
C_{23}^3&:(x_1,x_2,x_3)\to(x_1,x_2,x_3\oplus x_2)\equiv(3,4)(7,8),\\
C_{21}^3&:(x_1,x_2,x_3)\to(x_1\oplus x_2,x_2,x_3)\equiv(3,7)(4,8),\\
C_{32}^3&:(x_1,x_2,x_3)\to(x_1,x_2\oplus x_3,x_3)\equiv(2,4)(6,8),\\
C_{31}^3&:(x_1,x_2,x_3)\to(x_1\oplus x_3,x_2,x_3)\equiv(2,6)(4,8).
\end{aligned}\tag{4}$$

The Toffile (T^3) gate acts on three-bits and it is defined as follows, if the two control bits are set to 1 then the third target bit line is flipped. There are three possible T^3gates for the 3-in/out reversible circuits as shown in Fig.4.

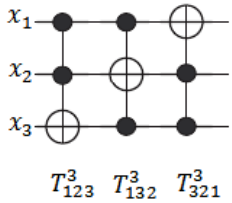

Figure 4: The 3 possible Toffoli (T) gates for 3-bit reversible circuits.

$$\begin{aligned}
T_{123}^3&:(x_1,x_2,x_3)\to(x_1,x_2,x_3\oplus x_1x_2)\equiv(7,8),\\
T_{132}^3&:(x_1,x_2,x_3)\to(x_1,x_2\oplus x_1x_3,x_3)\equiv(6,8),\\
T_{321}^3&:(x_1,x_2,x_3)\to(x_1\oplus x_2x_3,x_2,x_3)\equiv(4,8).
\end{aligned}\tag{5}$$

The M^3gate combines the action of the three gatesN, C and T^3andit acts on arbitrary 3-bits x_i, x_j and x_k in any order [18]. For 3-bit reversible circuits built using M-gate library, there are six possible M^3gates as shown in Fig.5, which perform as follows:

$$\begin{aligned}
M_{i,j,k}^3&:y_i=x_i\oplus(x_k\oplus x_j),\\
&\quad y_j=(x_j\oplus 1)\oplus(x_k\oplus x_j)\cdot\big(x_i\oplus(x_k\oplus x_j)\big),\\
&\quad y_k=x_k\oplus x_j,\\
M_{123}^3&:(x_1,x_2,x_3)\to(1,3,8,5,7,2,6,4),\\
M_{132}^3&:(x_1,x_2,x_3)\to(1,2,8,5,6,3,7,4),\\
M_{213}^3&:(x_1,x_2,x_3)\to(1,5,8,3,7,2,4,6),\\
M_{231}^3&:(x_1,x_2,x_3)\to(1,2,8,3,4,5,7,6),\\
M_{312}^3&:(x_1,x_2,x_3)\to(1,5,8,2,6,3,4,7),\\
M_{321}^3&:(x_1,x_2,x_3)\to(1,3,8,2,4,5,6,7).
\end{aligned}\tag{6}$$

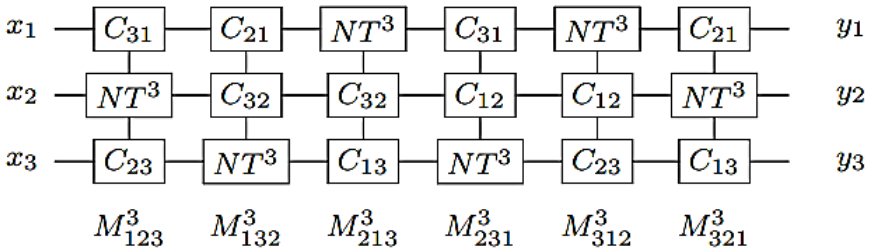

Figure 5: The 6 possibleM^3gates for 3-bit reversible circuits.

2.3 QUANTUM COST

The quantum cost of a reversible circuit refers to optimization measurement as the number of elementary gates required to build the reversible gate [21], i.e. the number of 2-qubit gates used in its implementation as a quantum circuit. In this paper, the cost of N gate is equal zero [15], and the cost of any 2-qubit gate is 1 and the quantum cost of M gate is equal 4 [18] as shown in Fig.6. The gate $[C_{23}v_{32}]$, which is merging gate between C_{23} and v_{32} in order, as shown in Fig.7. When implementing a reversible circuit, there are four elementary quantum gates that will be used: N gate, C gate, Controlled-$V(v)$ and Controlled-$V^+(u)$ gates, where $vu = uv = I$, $vv = uu = N$, and $I$is the identity gate [19].

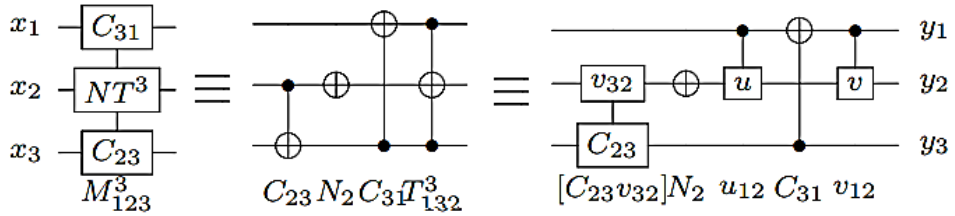

Figure 6: Decomposition of M^3 gate as 5 elementary gates (one of them with cost zero).

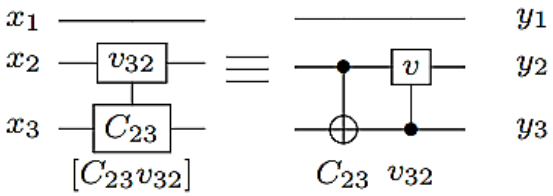

Figure 7: The circuit representation for the decomposition$[C_{23}v_{32}]$, of gate [17].

The N gate library added to the M^3gate library to form a new library called NM^3which is also universal [18]. The main NM^3library consists of nine gates (generators) as shown in Fig.8.

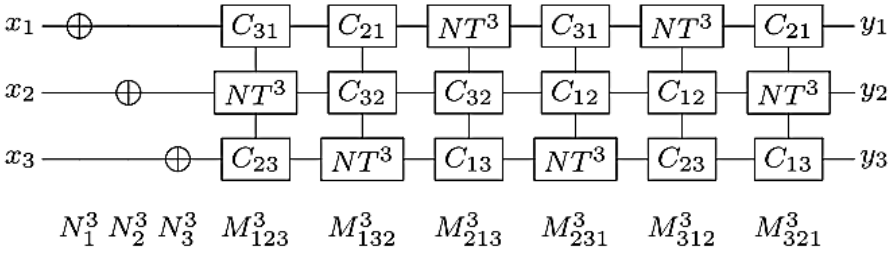

Figure 8: The main NM^3 library consist of 9 gates (generators)

III. Experimental Results

This section shows that if a set of Boolean operators can be integrated by an equivalent permutation that has a cycle representation, then the set of Boolean operators can be realized by a 3-bits reversible circuit based on NM^3 library.This gives concrete realizations for multiple families of Boolean functions such as $AND(x_1.x_2)$, $OR(x_1 + x_2)$, $NOT(\overline{x_1})$, $XOR(x_1 \oplus x_2)$, $NAND(\overline{x_1.x_2})$, $NOR(\overline{x_1 + x_2})$. For the sake of readability, this will be written shortly as $AND, OR, NOT, XOR, NAND\ and\ NOR$ respectively.

Among 20 different combinations, there exist 8 basic possible combinations of three different irreversible Boolean gates which are $\{\{AND, OR, NOT\}, \{AND, NOT, XOR\}, \{AND, NOT, NOR\}, \{OR, NOT, XOR\}, \{OR, NOT, NAND\}, \{NOT, XOR, NAND\}, \{NOT, XOR, NOR\}, \{NOT, NAND, NOR\}\}$ can be integrated by equivalent cyclic permutations as long as the integration maintains the reversibility. Each basic combination of three different irreversible Boolean functions has six possible permutations, and then we have a total of 48 possible combinations of three different irreversible Boolean functions. For example, the reversible circuit to implement the set $\{AND, NOT, XOR\}$ has six different forms, i.e. (XOR, NOT, AND) means that the first output line will be $XOR(x_1 \oplus x_2)$, the second output line will be $NOT(\overline{x_1})$ and the third line will be $AND(x_1.x_2)$ which is different from (AND, NOT, XOR) which means that the first output line will be $AND(x_1.x_2)$, the second output line be $NOT(\overline{x_1})$ and the third output line will be $XOR(x_1 \oplus x_2)$.

3.1 SETTING THE INPUT TO $(x_1, x_2, 0)$

This section discusses setting the input to $(x_1, x_2, 0)$, i.e. the third bit of a circuit is initialized to zero. Table.1 show NM^3-based reversible circuits with input $(x_1, x_2, 0)$ which are realized the 8 basic possible combinations of three different Boolean operators can be integrated by equivalent cyclic permutations, so that the integration provides the reversibility. For example, the combination of three different irreversible operators (XOR, NOT, AND) can be integrated by a cyclic permutation equal (1,3,7,2) and can be realized by reversible circuit $[M^3_{123}, N^3_1, M^3_{321}, M^3_{123}]$ with minimum cost equal 11 as shown in Fig.9.

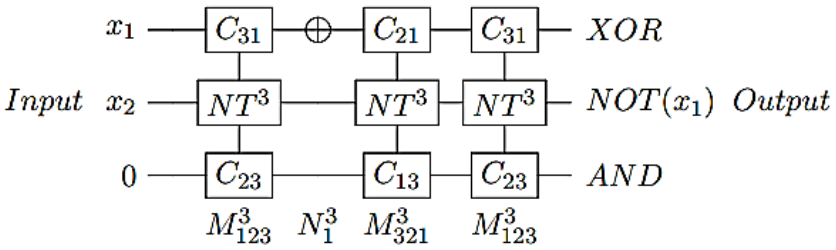

Figure 9: The NM^3-based reversible circuit realizes the combination of (XOR, NOT, AND) with the input $(x_1, x_2, 0)$.

3.2 SETTING THE INPUT TO $(x_1, x_2, 1)$

This section discusses setting the input to $(x_1, x_2, 1)$, i.e. the third bit of a circuit is initialized to one. Table.2 show NM^3-based reversible circuits with input $(x_1, x_2, 1)$ which are realized the 8 basic possible combinations of three different Boolean operators can be integrated by equivalent cyclic permutations so the integration keeps the reversibility of the circuit. For example, the combination of three different irreversible Boolean operators (XOR, NOT, AND) can be integrated by a cyclic permutation equal (2,3,4,7,8)(5,6) and can be realized by reversible circuit $[M^3_{321}, N^3_1, M^3_{312}, M^3_{321}, N^3_1, M^3_{321}]$ with minimum cost equal 16 as shown in Fig.10.

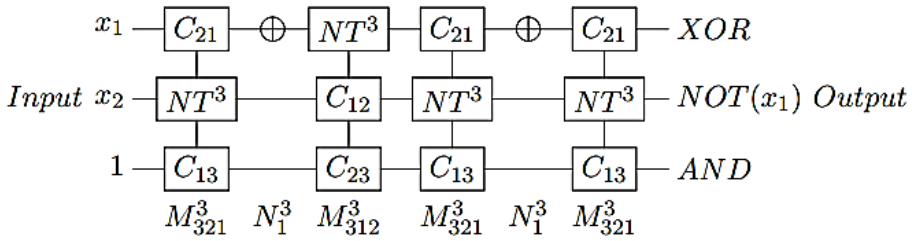

Figure 10: The NM^3-based reversible circuit realizes the combination of (XOR, NOT, AND) with the input $(x_1, x_2, 1)$.

Table 1: All the possible NM^3-based reversible circuits' realizations of Boolean operators' combination with input$(x_1, x_2, 0)$.

All-possible Combination	**Cyclic permutation**	**NM^3-based Reversible circuit**	**Quantum Cost [18]**	**Circuit Length**
(AND, OR, NOT)	(1,2)(3,4,5)	$[N_1^3, M_{213}^3, M_{321}^3, N_1^3, M_{213}^3, N_3^3]$	11	6
(AND, NOT, OR)	(1,3,4)(2,5)(6,7)	$[N_2^3, M_{123}^3, M_{123}^3, N_2^3, M_{231}^3, N_2^3, M_{231}^3]$	15	7
(OR, AND, NOT)	(1,2)(3,6)	$[M_{132}^3, M_{312}^3, M_{312}^3, M_{312}^3, N_2^3]$	15	5
(OR, NOT, AND)	(1,3,7,6)	$[M_{213}^3, M_{213}^3, N_1^3, M_{312}^3, N_1^3]$	11	5
(NOT, AND, OR)	(1,5,2)(3,6)(4,7)	$[M_{321}^3, N_3^3, M_{321}^3, N_3^3, M_{321}^3, M_{321}^3, N_3^3]$	15	7
(NOT, OR, AND)	(1,5,3,7,4)	$[M_{123}^3, N_2^3, M_{123}^3, M_{213}^3, N_2^3, M_{123}^3, N_2^3]$	15	7
(AND, NOT, XOR)	(1,3,4)(2,7,5)	$[M_{123}^3, M_{231}^3, N_2^3, M_{231}^3, M_{123}^3, N_1^3, N_2^3]$	14	7
(AND, XOR, NOT)	(1,2)(3,4,7,5)	$[N_1^3, M_{132}^3, N_1^3, N_3^3, M_{132}^3, N_1^3, M_{132}^3, N_3^3, M_{132}^3, N_3^3]$	16	10
(NOT, AND, XOR)	(1,5,2)(3,6,7)	$[M_{312}^3, N_3^3, M_{312}^3, N_1^3, M_{312}^3, M_{312}^3]$	16	6
(NOT, XOR, AND)	(1,5,3,7,2)	$[M_{312}^3, N_3^3, M_{312}^3, N_3^3, M_{312}^3, N_2^3, M_{312}^3, N_2^3, N_3^3]$	16	9
(XOR, AND, NOT)	(1,2)(3,6,7)	$[N_1^3, M_{132}^3, M_{231}^3, M_{132}^3]$	11	4
(XOR, NOT, AND)	(1,3,7,2)	$[M_{123}^3, N_1^3, M_{321}^3, M_{123}^3]$	11	4
(AND, NOT, NOR)	(1,4,7,5)	$[M_{213}^3, N_2^3, M_{213}^3, N_1^3, N_2^3, M_{213}^3, N_3^3]$	12	7
(AND, NOR ,NOT)	(1,4,7,5)(2,3)	$[M_{123}^3, M_{213}^3, M_{213}^3, M_{231}^3, N_1^3]$	15	9
(NOT, AND, NOR)	(1,6,7,3,5)	$[M_{123}^3, M_{123}^3, M_{213}^3, N_1^3, M_{123}^3, N_1^3]$	15	6
(NOT, NOR, AND)	(1,7,2,3,5)	$[N_1^3, M_{132}^3, N_1^3, M_{132}^3, M_{312}^3, N_1^3, M_{132}^3, N_1^3]$	15	8
(NOR, AND, NOT)	(1,6,5)(2,7,3	$[M_{132}^3, M_{132}^3, N_2^3]$	8	3
(NOR, NOT, AND)	(1,7,2,5)	$[N_2^3, M_{231}^3, M_{231}^3, N_2^3, N_3^3, M_{231}^3, N_1^3]$	12	7
(OR, NOT, XOR)	(1,3,8)(5,6,7)	$[M_{123}^3, N_1^3, M_{231}^3, M_{231}^3, N_1^3, M_{231}^3, N_1^3]$	15	7
(OR, XOR, NOT)	(1,2)(3,8)(5,7)	$[N_3^3, M_{321}^3, M_{213}^3, N_2^3, N_3^3, M_{213}^3]$	11	6
(NOT, OR, XOR)	(1,5,4)(3,8,7)	$[M_{312}^3, N_2^3, N_3^3, M_{312}^3, M_{312}^3, M_{312}^3, N_1^3, N_2^3]$	16	8
(NOT, XOR, OR)	(1,5,4)(2,7)(3,8)	$[N_1^3, M_{321}^3, N_1^3, N_3^3, M_{132}^3, M_{132}^3, N_1^3, M_{321}^3]$	15	8
(XOR, OR, NOT)	(1,2)(3,8,5,7)	$[M_{132}^3, N_1^3, N_2^3, M_{132}^3, N_1^3, M_{132}^3, M_{312}^3, N_1^3]$	15	8
(XOR, NOT, OR)	(1,3,8)(2,7)(5,6)	$[M_{132}^3, M_{312}^3, N_1^3, N_2^3, N_3^3]$	7	5
(OR, NOT, NAND)	(1,4)(3,8)(5,6,7)	$[N_1^3, M_{123}^3, M_{123}^3, N_2^3, M_{231}^3, N_2^3, M_{231}^3, N_1^3, N_2^3]$	15	9
(OR, NAND, NOT)	(1,4)(3,8)(5,7)	$[N_1^3, N_2^3, M_{123}^3, M_{123}^3, N_3^3, M_{123}^3, N_1^3, N_3^3]$	12	8
(NOT, OR, NAND)	(1,6)(3,8,7)(4,5)	$[N_1^3, M_{123}^3, M_{231}^3, N_1^3, N_2^3, M_{231}^3, N_2^3, M_{123}^3, N_1^3]$	14	9
(NOT, NAND, OR)	(1,7,2)(3,8)(4,5)	$[M_{132}^3, N_1^3, N_3^3, M_{132}^3, N_1^3, N_3^3, M_{132}^3, M_{132}^3, N_3^3]$	16	9
(NAND, OR, NOT)	(1,6)(3,8,5,7)	$[N_1^3, M_{123}^3, N_2^3, M_{213}^3, N_2^3]$	7	5
(NAND, NOT, OR)	(1,7,2)(3,8)(5,6)	$[N_2^3, M_{123}^3, N_1^3, M_{132}^3, N_1^3, N_2^3]$	8	6
(NOT,XOR, NAND)	(1,6,7)(3,8)(4,5)	$[N_3^3, M_{321}^3, N_1^3, N_3^3, M_{321}^3, N_1^3, N_3^3, M_{321}^3, N_3^3, M_{321}^3, N_1^3]$	16	11
(NOT, NAND, XOR)	(1,7)(3,8)(4,5)	$[N_1^3, M_{123}^3, N_1^3, N_2^3, M_{213}^3, N_1^3, N_2^3, M_{213}^3]$	12	8
(XOR, NOT, NAND)	(1,4,7)(3,8)(5,6)	$[N_1^3, N_2^3, M_{123}^3, N_1^3, M_{312}^3, N_2^3, M_{123}^3, M_{123}^3, N_1^3]$	15	9
(XOR, NAND, NOT)	(1,4,5,7)(3,8)	$[N_2^3, M_{213}^3, M_{312}^3, M_{312}^3, N_2^3, M_{213}^3, N_2^3]$	14	7
(NAND,NOT,XOR)	(1,7)(3,8)(5,6)	$[N_3^3, M_{231}^3, N_3^3, M_{231}^3, N_3^3, M_{231}^3]$	12	6
(NAND,XOR,NOT)	(1,6,5,7)(3,8)	$[N_3^3, M_{123}^3, M_{123}^3, N_3^3, M_{123}^3, N_3^3, M_{231}^3]$	15	7
(NOT,XOR,NOR)	(1,6,5,3,7)	$[M_{123}^3, M_{123}^3, M_{213}^3, M_{123}^3, N_2^3]$	15	5
(NOT, NOR,XOR)	(1,7)(2,5)(3,6)	$[M_{213}^3, M_{132}^3, N_2^3, M_{132}^3, N_2^3]$	11	5
(XOR, NOT, NOR)	(1,4,3,7)	$[M_{213}^3, M_{231}^3, N_3^3, M_{213}^3, N_3^3]$	11	5
(XOR, NOR, NOT)	(1,4,7)(3,6)	$[N_2^3, M_{312}^3, N_2^3, M_{123}^3, M_{123}^3]$	11	5
(NOR, NOT, XOR)	(1,7)(2,5)(3,4)	$[N_2^3, M_{231}^3, M_{231}^3, N_3^3, M_{231}^3, N_1^3, N_2^3]$	12	7
(NOR, XOR, NOT)	(1,6,7)(3,4,5)	$[N_1^3, M_{132}^3, N_1^3, M_{132}^3, M_{132}^3, N_1^3, M_{132}^3, N_1^3]$	16	8
(NOT,NAND, NOR)	(1,8,5,3,7)	$[N_2^3, M_{132}^3, N_1^3, M_{132}^3, M_{312}^3, N_1^3, M_{132}^3, N_2^3]$	15	8
(NOT,NOR, NAND)	(1,8,7)(2,5)(3,6)	$[N_1^3, M_{123}^3, N_1^3, M_{213}^3, M_{123}^3, N_1^3, M_{123}^3, N_1^3]$	15	8
(NAND,NOT, NOR)	(1,8,3,7)	$[N_3^3, M_{231}^3, N_3^3, M_{231}^3, N_2^3, N_3^3, M_{231}^3, N_2^3]$	12	8
(NAND,NOR, NOT)	(1,8,7)(3,6)	$[N_2^3, M_{213}^3, M_{213}^3, M_{213}^3, N_2^3, M_{213}^3, M_{213}^3, N_2^3]$	20	8
(NOR,NOT, NAND)	(1,8,7)(2,5)(3,4)	$[N_1^3, M_{123}^3, N_1^3, M_{123}^3]$	8	4
(NOR,NAND, NOT)	(1,8,7)(3,4,5)	$[M_{123}^3, N_1^3, M_{321}^3, N_1^3, M_{321}^3, M_{123}^3, N_1^3]$	14	7

Table 2: All the possible NM^3-based reversible circuits' realizations of Boolean operators'combination with input$(x_1, x_2, 1)$.

All-possible Combination	**Cyclic permutation**	**NM^3-based Reversible circuit**	**Quantum Cost [18]**	**Circuit Length**
(AND, OR, NOT)	(3,6)(7,8)	$[M^3_{312}, N^3_2, M^3_{123}, M^3_{123}, M^3_{213}]$	15	5
(AND, NOT, OR)	(2,3,8,6)	$[N^3_1, M^3_{213}, N^3_1, \mathrm{N}^3_2, M^3_{213}, N^3_1, N^3_2, M^3_{231}]$	12	8
(OR, AND, NOT)	(4,6,5)(7,8)	$[N^3_1, M^3_{213}, M^3_{321}, N^3_1, M^3_{213}]$	11	5
(OR, NOT, AND)	(2,3)(4,7)(5,8,6)	$[M^3_{123}, M^3_{123}, N^3_2, M^3_{231}, N^3_1, M^3_{231}, N^3_1, N^3_2]$	15	8
(NOT, AND, OR)	(2,5,8,4,6)	$[M^3_{123}, M^3_{231}, M^3_{321}, N^3_2, M^3_{312}]$	15	5
(NOT, OR, AND)	(2,5)(3,6)(4,7,8)	$[M^3_{123}, M^3_{312}, M^3_{132}, M^3_{312}, N^3_1]$	15	5
(AND, NOT, XOR)	(2,3,6)(5,8)	$[M^3_{312}, N^3_2, M^3_{213}, N^3_2, M^3_{123}]$	11	5
(AND, XOR ,NOT)	(3,6)(5,8)	$[N^3_3, M^3_{123}, M^3_{321}, N^3_2, M^3_{123}]$	11	5
(NOT, AND, XOR)	(2,5,4,6)(3,8)	$[N^3_1, M^3_{231}, M^3_{231}, M^3_{321}, M^3_{321}]$	15	5
(NOT, XOR, AND)	(2,5,4,7,8)(3,6)	$[N^3_1, N^3_2, M^3_{123}, N^3_1, M^3_{312}, M^3_{312}, N^3_2, N^3_3]$	11	8
(XOR, AND, NOT)	(3,8)(4,6,5)	$[N^3_3, M^3_{123}, N^3_3, M^3_{312}, N^3_3, M^3_{312}]$	11	6
(XOR, NOT, AND)	(2,3,4,7,8)(5,6)	$[M^3_{321}, N^3_1, M^3_{312}, M^3_{321}, N^3_1, M^3_{321}]$	16	6
(AND, NOT, NOR)	(1,6)(2,4,3)(5,8)	$[N^3_3, M^3_{321}, M^3_{321}, M^3_{231}, M^3_{231}]$	15	5
(AND, NOR ,NOT)	(1,6)(2,4)(5,8)	$[N^3_2, M^3_{123}, N^3_2, M^3_{123}, \ N^3_2, M^3_{123}]$	12	6
(NOT, AND, NOR)	(1,2,6)(3,8)(4,5)	$[N^3_1, M^3_{132}, M^3_{321}, N^3_1, M^3_{321}, M^3_{321}]$	15	6
(NOT, NOR, AND)	(1,4,2,6)(3,8)	$[N^3_1, M^3_{132}, \ N^3_1, M^3_{132}, \ N^3_1, N^3_3, M^3_{132}, M^3_{132}, N^3_1, N^3_2]$	16	10
(NOR, AND, NOT)	(1,6)(2,7,8)(4,5)	$[M^3_{123}, M^3_{213}, N^3_1, N^3_3]$	7	4
(NOR, NOT, AND)	(1,6)(2,7,8)(3,4)	$[N^3_1, N^3_3, M^3_{123}, N^3_1, M^3_{123}, N^3_3]$	8	6
(OR, NOT, XOR)	(2,3)(4,8,5)	$[M^3_{312}, N^3_1, N^3_2, M^3_{213}, N^3_2, M^3_{123}, N^3_1, N^3_2]$	11	8
(OR, XOR, NOT)	(4,8,5)(6,7)	$[M^3_{213}, N^3_2, N^3_3, M^3_{312}, N^3_2, M^3_{123}]$	11	6
(NOT, OR, XOR)	(2,5)(3,6,4,8)	$[N^3_1, N^3_2, M^3_{132}, N^3_2, M^3_{132}, M^3_{321}, N^3_2, M^3_{321}, N^3_1]$	15	9
(NOT, XOR, OR)	(2,5,6,4,8)	$[N^3_2, M^3_{123}, M^3_{312}, N^3_2, M^3_{312}, M^3_{312}]$	15	6
(XOR, OR, NOT)	(3,4,8)(6,7)	$[N^3_1, M^3_{213}, M^3_{213}, M^3_{213}, N^3_1, N^3_2]$	12	6
(XOR, NOT, OR)	(2,3,4,8)	$[N^3_1, M^3_{213}, N^3_1, N^3_2, M^3_{213}, N^3_1, M^3_{213}, N^3_2]$	12	8
(OR, NOT, NAND)	(2,4,8,5)	$[N^3_2, M^3_{213}, N^3_1, N^3_2, M^3_{213}, N^3_1, N^3_2, M^3_{231}, N^3_1, N^3_2]$	12	10
(OR, NAND, NOT)	(2,4,8,5)(6,7)	$[N^3_1, N^3_2, M^3_{123}, M^3_{312}, N^3_1, M^3_{123}, N^3_2, M^3_{123}, N^3_1]$	15	9
(NOT, OR, NAND)	(2,6,4,8,3)	$[N^3_2, M^3_{132}, N^3_1, M^3_{213}, N^3_2, M^3_{132}, N^3_2, M^3_{132}, N^3_1]$	15	9
(NOT, NAND, OR)	(2,7,6,4,8)	$[N^3_1, M^3_{123}, N^3_2, M^3_{213}, M^3_{213}, N^3_2, M^3_{213}, N^3_1]$	15	8
(NAND, OR, NOT)	(2,6,7)(3,4,8)	$[N^3_1, M^3_{132}, N^3_2, M^3_{132}, N^3_1]$	8	5
(NAND, NOT, OR)	(2,7,4,8)	$[M^3_{231}, N^3_3, M^3_{231}, N^3_2, N^3_3, M^3_{231}, N^3_2, N^3_3]$	12	8
(NOT, XOR, NAND)	(1,2,6,4,8)	$[N^3_3, M^3_{312}, N^3_3, M^3_{312}, N^3_3, M^3_{312}, N^3_2, M^3_{312}, N^3_2]$	16	9
(NOT, NAND, XOR)	(1,6,4, 8)(2,7)	$[M^3_{123}, N^3_2, M^3_{231}, N^3_3, M^3_{312}, N^3_2, M^3_{231}]$	14	7
(XOR, NOT, NAND)	(1,2,4,8)	$[N^3_3, M^3_{123}, N^3_1, M^3_{321}, M^3_{123}, N^3_3]$	11	6
(XOR, NAND, NOT)	(1,2,4,8)(6,7)	$[N^3_1, M^3_{123}, N^3_1, M^3_{213}, N^3_1, M^3_{213}, M^3_{213}]$	15	7
(NAND, NOT, XOR)	(1,4,8)(2,7)	$[M^3_{312}, N^3_1, M^3_{312}, N^3_2, M^3_{123}, N^3_2]$	11	6
(NAND, XOR, NOT)	(1,4,8)(2,6,7)	$[N^3_3, M^3_{123}, N^3_3, M^3_{312}, M^3_{123}, N^3_3, M^3_{312}, N^3_3]$	15	8
(NOT, XOR, NOR)	(1,8)(2,6,3)(4,7)	$[N^3_1, N^3_3, M^3_{321}, M^3_{132}, N^3_3, M^3_{132}, N^3_1, M^3_{321}]$	14	8
(NOT, NOR, XOR)	(1,8)(2,7,4,6)	$[N^3_1, N^3_3, M^3_{312}, M^3_{231}, N^3_1, N^3_3, M^3_{123}, M^3_{231}]$	14	8
(XOR,NOT, NOR)	(1,8)(2,4,7)(5,6)	$[N^3_3, M^3_{132}, M^3_{312}, N^3_1, N^3_2]$	7	5
(XOR, NOR, NOT)	(1,8)(2,4,6,5)	$[N^3_2, M^3_{213}, M^3_{213}, N^3_1, M^3_{213}, M^3_{213}, N^3_1, M^3_{213}, M^3_{213}]$	24	9
(NOR,NOT,XOR)	(1,8)(2,7,6)	$[M^3_{312}, M^3_{312}, N^3_2, M^3_{123}, N^3_1]$	11	5
(NOR, XOR, NOT)	(1,8)(2,6,3)	$[N^3_1, M^3_{213}, M^3_{213}, N^3_2, M^3_{132}, N^3_1, N^3_2]$	11	7
(NOT, NAND, NOR)	(1,2,8)(3,6)(4,7)	$[N^3_3, M^3_{132}, N^3_1, N^3_3, M^3_{312}, N^3_1, N^3_3, M^3_{132}, M^3_{132}]$	16	9
(NOT, NOR, NAND)	(1,4,6,2,8)	$[N^3_2, M^3_{123}, N^3_2, M^3_{213}, M^3_{213}, N^3_2, M^3_{213}, N^3_2]$	15	8
(NAND, NOT, NOR)	(1,2,8)(4,7)(5,6)	$[M^3_{123}, N^3_1, N^3_3, M^3_{123}, N^3_1, N^3_3]$	8	6
(NAND, NOR, NOT)	(1,2,8)(4,6,5)	$[M^3_{123}, M^3_{321}, M^3_{123}, M^3_{321}, N^3_1]$	14	5
(NOR, NOT, NAND)	(1,6,2,8)	$[N^3_1, M^3_{213}, N^3_1, M^3_{231}, N^3_1, M^3_{231}, N^3_1]$	11	7
(NOR, NAND, NOT)	(1,2,8)(3,6)	$[M^3_{312}, M^3_{312}, N^3_1, N^3_3, M^3_{312}, M^3_{312}, N^3_3, M^3_{312}]$	20	8

3.3 COMPARISON BETWEEN SETTING THE INPUTS $(x_1, x_2, 0)$ AND $(x_1, x_2, 1)$

Table.3 shows that the comparison between the possible combinations of Boolean operators which realize the NM^3 -based reversible circuits with minimum cost and length while the inputs $(x_1, x_2, 0)$and$(x_1, x_2, 1)$. Initializing the input vector to $(x_1, x_2, 0)$ gives better results with respect to the average quantum cost, having cost of 9.25 and the average length, having length of 4.62 as shown in Table.3.

Table 3: Comparison between the possible combinations of Boolean operators which realize the NM^3-based reversible circuits' with minimum cost and length while the inputs $(x_1, x_2, 0)$ and$(x_1, x_2, 1)$.

Input $(x_1, x_2, 0)$			
Basic Combinations	NM^3-based Reversible Circuits	Mini-Cost	Length
(OR, NOT,AND)	$[M_{213}^3, M_{213}^3, N_1^3, M_{312}^3, N_1^3]$	11	5
(XOR ,NOT,AND)	$[M_{123}^3, N_1^3, M_{321}^3, M_{123}^3]$	11	4
(NOR,AND,NOT)	$[M_{132}^3, M_{132}^3, N_2^3]$	7	3
(XOR, NOT,OR)	$[M_{132}^3, M_{312}^3, N_1^3, N_2^3, N_3^3]$	7	5
(NAND,OR,NOT)	$[N_1^3, M_{123}^3, N_2^3, M_{213}^3, N_2^3]$	7	5
(NAND,NOT,XOR)	$[N_3^3, M_{231}^3, N_3^3, M_{231}^3, N_3^3, M_{231}^3]$	12	6
(NOT, NOR, XOR)	$[M_{213}^3, M_{132}^3, N_2^3, M_{132}^3, N_2^3]$	11	5
(NOR,NOT,NAND)	$[N_1^3, M_{123}^3, N_1^3, M_{123}^3]$	8	4
Average		9.25	4.62
Input $(x_1, x_2, 1)$			
Basic Combinations	NM^3-based Reversible Circuits	Mini-Cost	Length
(OR, AND, NOT)	$[N_1^3, M_{213}^3, M_{321}^3, N_1^3, M_{213}^3]$	11	5
(XOR, NOT,AND)	$[M_{321}^3, N_1^3, M_{312}^3, M_{321}^3, N_1^3, M_{321}^3]$	16	6
(NOR, AND,NOT)	$[\mathrm{M}_{123}^3, \mathrm{M}_{213}^3, \mathrm{N}_1^3, \mathrm{N}_3^3]$	7	4
(OR, XOR, NOT)	$[\mathrm{M}_{213}^3, \mathrm{N}_2^3, \mathrm{N}_3^3, \mathrm{M}_{312}^3, \mathrm{N}_2^3, \mathrm{M}_{123}^3]$	11	6
(NAND, OR, NOT)	$[\mathrm{N}_1^3, \mathrm{M}_{132}^3, \mathrm{N}_2^3, \mathrm{M}_{132}^3, \mathrm{N}_1^3]$	8	5
(NAND, XOR,NOT)	$[\mathrm{N}_3^3, \mathrm{M}_{123}^3, \mathrm{N}_3^3, \mathrm{M}_{312}^3, \mathrm{M}_{123}^3, \mathrm{N}_3^3, \mathrm{M}_{312}^3, \mathrm{N}_3^3]$	15	8
(NOT, NOR, XOR)	$[\mathrm{N}_1^3, \mathrm{N}_3^3, \mathrm{M}_{312}^3, \mathrm{M}_{231}^3, \mathrm{N}_1^3, \mathrm{N}_3^3, \mathrm{M}_{123}^3, \mathrm{M}_{231}^3]$	14	8
(NAND, NOT,NOR)	$[\mathrm{M}_{123}^3, \mathrm{N}_1^3, \mathrm{N}_3^3, \mathrm{M}_{123}^3, \mathrm{N}_1^3, \mathrm{N}_3^3]$	8	6
Average		11.25	5.88

IV. Conclusion

Classical Boolean gates are mainly irreversible and cannot be used directly in the reversible circuits' synthesis. Methods to integrate any three Boolean operators, so that the integration keeps the reversibility, as a NM^3-based reversible circuit with zero-garbage output have been proposed. It was shown that the order of the Boolean operator in the output vector affects the efficiency of the circuit. There are two ways to initialize the input vectors $(x_1, x_2, 0)$ and $(x_1, x_2, 1)$. It was shown that setting the input vector to$(x_1, x_2, 0)$ of the NM^3-based reversible circuits gives better results with respect to the average quantum cost, having cost of 9.25 and the average length, having length of 4.62.

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