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Self-adjusting Fast Trim and Trim Verification Solution for Hi-sensitive Integrated Sensor Circuit

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ABSTRACT: *This article describes a fast, low-cost solution for a sequential, self-adjusting OTP(One-TimeProgramming) and programming verification of Zener diodes on a hi-sensitive integrated sensor circuit. If we select the proper structures of Zener diodes (also known as 'Zener-zap') in a standard CMOS(Complementary Metal–Oxide–Semiconductor)process, it enables us to achieve better accuracy in high-precision integrated circuits. For this purpose, we developed a solution for fast programming and programming verification of 500 Zener-zap structures on the sensor ASIC (Application Specific Integrated Circuit). This solution we implemented for wafer sorting and as well for packaged parts. Such an approach is necessary to eliminate small performance changes due to stress caused by handling the sensors before they are placed in the final package. After fine-trimming several crucial parameters of the sensor, we do the pre-specified functionality test of the entire sensor. We store measurement data, including OTP verification measurements, in an STDF (Standard Test Data Format) file for later statistical evaluation.*

KEYWORDS –*Self-adjusting, One-Time Programming, Zener-zap, Anti-fuse, STDF*

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I. INTRODUCTION

In the modern industry, plenty of high-precision, low-cost, fully integrated analog sensors are necessary. Over the years, several methods have been discovered to overcome the tolerances of the integrated circuit fabrication process. Although known ratiometric design principles may be successfully adopted, there is still a need for more precise methods to adjust the most critical parameters of the integrated sensors. We can use different OTP methods. The most common are laser trimming, poly fuse burning, and Zener-zapping. Using these methods, we can significantly improve the production yield and fulfill the requirements for the accuracy of high-precision demands for integrated sensors.

This article describes a one-time programming technique that uses Zener-zapping. This quite well-established method creates anti-fuse devices where they are needed. The term 'anti-fuse' describes an element which initially represents an open circuit but can be later irreversibly changed, to approach to a short circuit. We can create such a structure with a reverse-biased Zener diode – a small, subsurface lateral N+, P+ structure. A temporary avalanche breakdown in a P-N junction occurs when we increase the Zener diode programming current. This avalanche breakdown causes localized heating and subsequent migration of metallization across the junction (spiking). In other words, Zener-zapping is a short current pulse to the reverse-biased Zener diode. The OTP drastically changes the resistance of the zapped diode. This fascinating process is described in more detail in [1] and [2].

Additional improvements to OTP methods represent articles [3] and [4]. We see the trend in further increasing reliability while reducing the zapping current. This article presents our fast, self-adjusting method of OTP. We verified this approach during the last few years by trimming more than ten million of high-precision, integrated sensors.

II. FAST, SELF-ADJUSTING OTP SOLUTION

We developed a sophisticated, high-precision, an application-specific magnetic sensor in our Laboratory of Microelectronics at the Faculty of Electrical Engineering. Fig. 1 presents an actual photograph of a small part of the Zener-zap array on our ASIC. This photograph of four Zener-zap structures we took at 3000x magnification. For shooting this photo, some layers above the Zener-zap structures had to be etched away. Unfortunately, in the micro-world, the entire Zener zap structure is not perfectly level. So some parts of the picture are somewhat out of focus at this magnification. Here we used widely available and proven OTP Zener-zap cells from the silicon foundry technology library. In general, very little information is available on implementing the fast zapping procedure for such specific cells. When we started to deal with the OTP topic, we experienced quite a few difficulties in achieving a quick and consistent Zener-zapping. A wrong pulse size or current may cause insufficient migration of metallization across the junction. In this case, evident OTP

programming may even erase in a relatively short time. We soon realized that other teams also had much trouble with OTPand that our assistance was welcome.

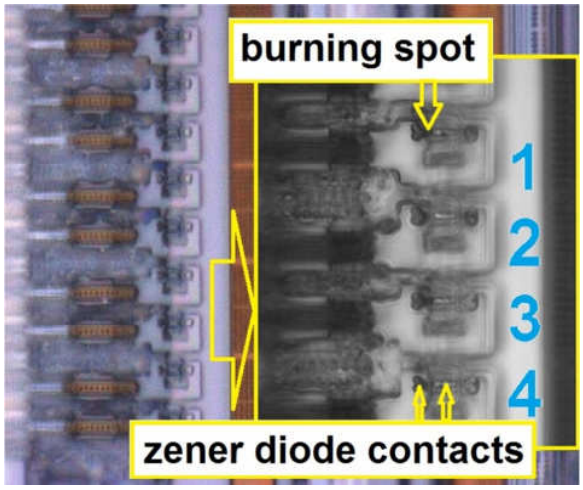

Figure 1: Four Zener-zap structures photograph taken at 3000x magnification.

The standard method for Zener-zapping is to discharge a small capacitor over a reverse-biased Zener diode. This method forces a pretty well-defined and repeatable avalanche breakdown in a P-N junction. When properly selected, we can quickly achieve the desired pulse width from 1 µs to 3 µs [2]. The problem is that this method needs some extra time to sufficiently recharge the capacitor. A drawback is also evident that during the programming, we must disconnect the charging current from the discharging capacitor. This switching additionally slows down the time effectiveness of this method.

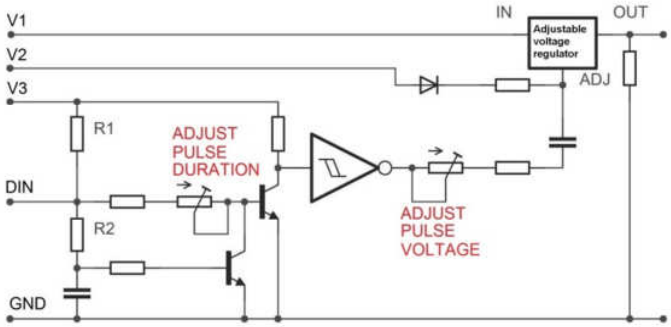

Figure 2: Simplified schematic for the generation of variable OTP pulse.

Another approach is to use expensive dedicated equipment that is capable of driving and precisely controlling the current and pulse shape for a relatively short burn pulse (approximately one microsecond). We got an invitation to compare the results from our low-cost solution with a similar solution running on such relatively expensive equipment (approximate cost ratio to ours is 1:50). Our solution was superior.

Fig.2 describes the method proposed in this article. The analog output V2 controls the adjustable voltage regulator with a goal, to achieve different levels of the pulse-train. Pulse-train is used as a clock to address each of the 500 Zener-zap cells [5]. The change of the DIN digital input signal level triggers the OTP pulse. Delay circuit briefly triggers a Schmitt trigger. This signal adds an OTP pulse to the pulse train via a small capacitor. By changing the resistivity, we can adjust the pulse duration and the pulse voltage. To achieve the time of approximately one-microsecond pulse duration, a resistor R2 must have a way bigger resistance value than resistor R1. Voltage V1 must be at least a few millivolts higher than the allowed maximum programming voltage. Voltage V3must equal to 5 volts for proper Schmitt trigger operation. A detailed example of such a pulse we show in Fig.3. As we can see, we preserved the desired positive part of the triggered glitch, and we also almost eliminated the undesired negative part. This feature is essential for stable communication with the ASIC. The best OTP results were usually achieved at a pulse time a little bit below one microsecond, with a pulse peak of 8.25 V, and at 6.75 V signal level remaining after the glitch.

The criterion for these three parameters is the statistical analysis of zapped fuse resistance uniformity. When the consistency is high, we are close to the ideal zapping parameters. For different wafer lots or even different wafers within one lot, these values can be slightly different. The self-adjustingZener-zapping algorithm selects one chip on a silicon wafer and burns all 500 Zener-zap fuses with somewhat different parameters. By evaluating the resistances of the burned Zener-zap structures, it proposes the optimal settings and stores them to the configuration file. So we have automatically generated the most suitable Zener-zapping settings for each wafer lot.

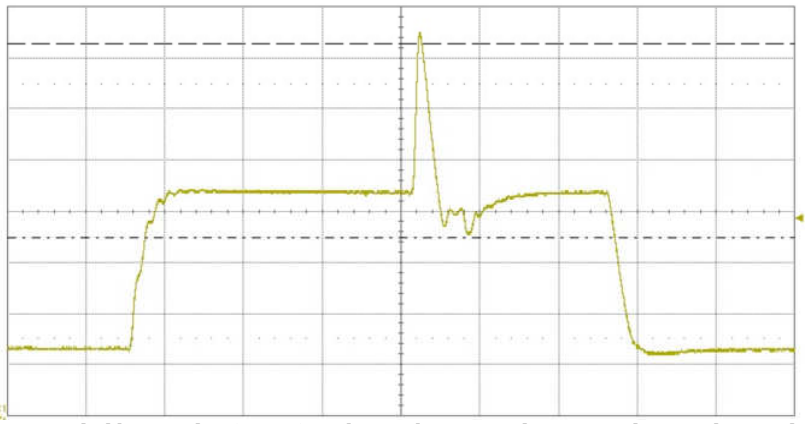

Figure 3: Detailed burn pulse (8.27V) with time base 2 μs/division and vertical 0.5V/division.

III. CREATION OF THE STDF FILE

If we want to track back each device and compare the on-wafer measurements with later measurements of the packaged parts, we need to store a considerable amount of test measurement data. For this purpose, we used the STDF format. STDF is a proprietary file format for semiconductor test information, initially developed by Teradyne, as a test result output of all of Teradyne UNIX operating system based testers. Teradyne derives no direct commercial benefit from propagating this standard. Now it is widely used throughout the semiconductor industry since it is a commonly employed format. Automatic test equipment platforms from all leading manufacturers nowadays have also the possibility to produce an STDF output file. STDF is a binary file format. Bulky specifications are freely available on the internet.

The more natural way to create a binary STDF file is to create a standard ATDF (ASCII Test Data format) file first. Standard ATDF file specifications are also freely available on the internet. Fortunately, there are also some tools freely available on the web that will do the conversion from ATDF to STDF and vice versa. They do not lose any information in this process. As usual, the ATDF specification is also quite extensive, and it takes quite some time to determine the required sequence of the necessary record types. So let us give some guidelines about the accepted series of the ATDF record types:

1. The first record type should be “FAR” (File Attributes Record). It determines ATDF and STDF format versions and scaling flag.
2. “ATR” (Audit Trail Record) is second record type, and it is necessary to record all operations essential to the contents of the file.
3. “MIR” (Master Information Record) record is needed for all global information of the file.
4. “SDR” (Site Description Record) describes the presence of test sites and test heads.
5. Then we may have several “PMR” (Pin Map Record) type records.
6. “PGR” (Pin Group Record) is used to associate a pin name with a group of pins.
7. “WIR” (Wafer Information Record) is used to mark the beginning of the wafer test.
8. “PIR” (Part Information Record) acts as a marker to indicate where testing of a particular DUT (Device under Test) started. It precedes the “BPS” (Begin Program Section Record) type record. Then we can have several “PTR” (Parametric Type Record), “FTR” (Functional Type Record), and other similar record types to store measurement data. After all measurement data for one DUT is stored, we insert the “EPS” (End Program Section Record) record type. The last record type is “PRR” (Part Result Record) that contains the results information relating to each part tested by the test program. We repeat step 8 for all tested parts.
9. Then we have all the necessary “TSR” (Test Synopsis Record) type records. They contain statistics for one parametric or functional test.

10. After the "TSR" type record, we may have several "HBR" (Hardware Bin Record) type records. They store a count of parts placed in a particular bin after testing. Here we may have "pass" or "fail" or similar "bins" we use.
11. "PCR" (Part Count Record) type record includes part count totals for one or all test sites.
12. "WRR" (Wafer Results Record) type record includes results for each wafer tested by the test program.
13. "MRR" (Master Results Record) is the last type record in the ATDF file and is a logical extension of the "MIR" type record.

The above 13 points describe the ATDF file structure. After we have successfully generated the standard ATDF file, we may use freely available internet tools to create a valid STDF file. This file we can later use for automatic statistical analysis for the entire population of tested devices. Usually, one STDF file per silicon wafer is required, but we may also join results from several wafers into one STDF file.

IV. CONCLUSION

In most mixed-mode integrated circuits nowadays dominates a reliable digital part area. Failing a small analog portion to meet strict, predefined accuracy requirements can cause poor yield economics issues. Adopting efficient trimming of critical parameters is more than welcome - especially when relatively large quantities of expensive silicon are in question.

Besides yield, test time optimization is also very essential. The method, presented in this paper, successfully eliminates the drawback of slow capacitor recharging, and we can repeat the burning in the range of microseconds. With the described OTP method, the trimming time of 500Zener zaps takes approximately seven milliseconds. Time here is a little longer than necessary to increase the reliability of the 'on-chip' integrated communication protocol. The test system itself would accomplish the zapping task even faster.

Another benefit of the described method is that the entire pulse train shape can be easily readjusted and adapted to a specific wafer or wafer lot automatically by the software itself. Quite notable is also the fact that we expect no lifetime reliability problems of properly trimmed Zener zaps. The reason for this we can also see in Fig. 1. During OTP, we cause no physical damage to the passivation or other layers below the silicon wafer surface. So, all the affected structures remain safely isolated from the harsh outer environmental influences. Here we mean sawing, dicing, and packaging of the devices.

We implemented this solution for wafer sorting and also packaged parts sorting. As mentioned early in the text, the purpose of this OTP solution development was to test in our laboratory designed ASIC with a high-precision magnetic sensor. We successfully verified this OTP method in the industrial production of more than ten million high precision electronic micro-systems.

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