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# 2-Bit Magnitude Comparator Design Using Different Logic Styles

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**ABSTRACT:** *2-bit magnitude comparator design using different logic styles is proposed in this brief. Comparison is most basic arithmetic operation that determines if one number is greater than, equal to, or less than the other number. Comparator is most fundamental component that performs comparison operation. This brief presents comparison between different logic styles used to design 2-Bit magnitude comparator. Comparison between different designs is calculated by simulation that is performed at 90nm technology in Tanner EDA Tool.*

**Keywords —** *Binary comparator, digital arithmetic, high-speed, low power.*

## 1. INTRODUCTION

In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number [1]. So comparator is used for this purpose. Magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes (Fig.1). The outcome of comparison is specified by three binary variables that indicate whether **A>B, A=B, or A<B.**

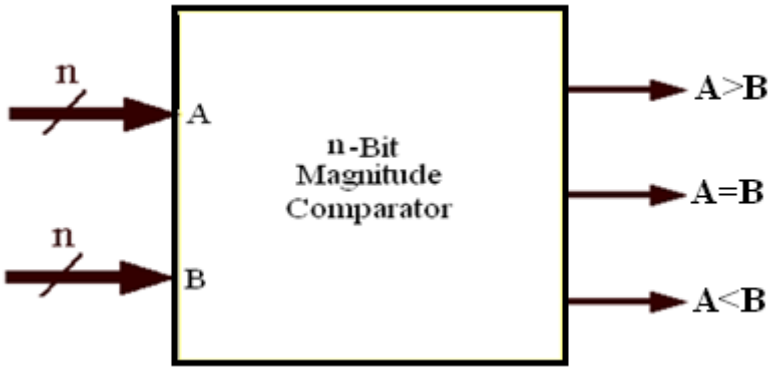



**Figure 1. Block Diagram of n-Bit Magnitude Comparator**

The circuit, for comparing two n-Bit numbers, has 2n inputs & $2^{2n}$ entries in the truth table, for 2-Bit numbers, 4-inputs & 16-rows in the truth table, similarly, for 3-Bit numbers 6-inputs & 64-rows in the truth table [2].

The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. Circuit size depends on the number of transistors and their sizes and on the wiring complexity. The wiring complexity is determined by the number of connections and their lengths. All these characteristics may vary considerably from one logic style to another and thus proper choice of logic style is very important for circuit performance [3], [4].

In order to differentiate all four designs, simulations are carried out for power, Delay, Power Delay Product at varying supply voltages from 0.6v to 1.4v in step of 0.2v. Simulations are performed at 90nm technology in Tanner EDA Tool.

## 2. 2-BIT MAGNITUDE COMPARATOR

2-Bit Magnitude Comparator Compares two numbers each having two bits (A1, A0 & B1, B0). For this arrangement truth table [5] has 4 inputs & 16 entries as in **Table 1**.

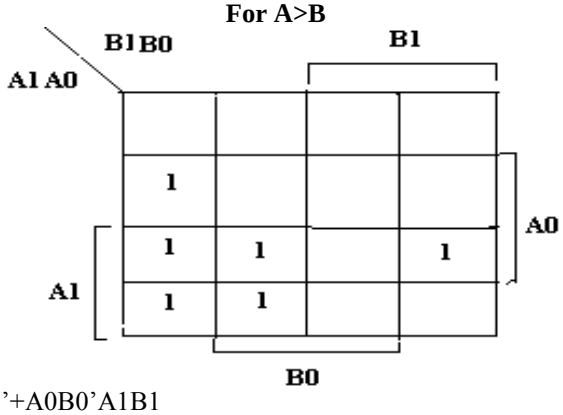
**Table 1. Truth Table of 2-Bit Magnitude Comparator**

| INPUT | | | | OUTPUT | | |
|---|---|---|---|---|---|---|
| **A1** | **A0** | **B1** | **B0** | **A>B** | **A=B** | **A<B** |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

## 2.1 Karnaugh Mapping

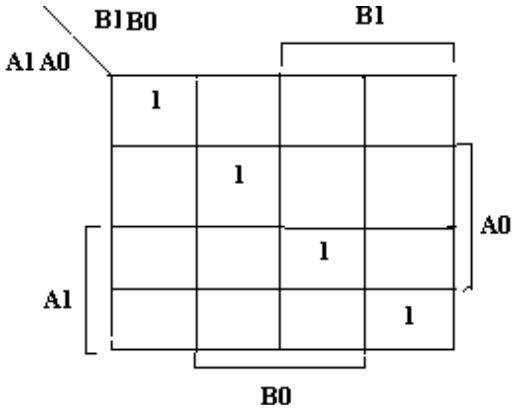
K-Map is used to minimize Boolean function obtained from truth table [5].

**For A>B**

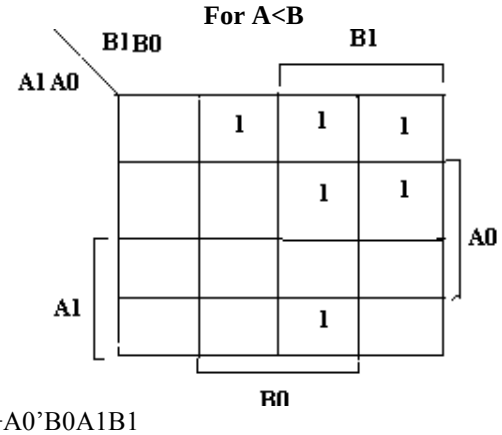



A>B: = A1B1'+A0B0'A1'B1'+A0B0'A1B1
= A1B1'+A0B0'(A1'B1'+A1B1)
= A1B1'+A0B0' X1

**For A=B**




A=B: = A1'A0'B1'B0'+ A1'A0B1'B0+A1A0'B1B0'+A1A0B1B0
= (A1'B1'+A1B1) (A0'B0'+A0B0)
= X1X0




A<B: = A1'B1+A0'B0A1'B1'+A0'B0A1B1
= A1'B1+A0'B0(A1'B1'+A1B1)
= A1'B1+A0'B0 X1

## 2.2 Logic Diagram

According to logic function obtained from truth table, logic diagram is drawn as in **Fig.2:**

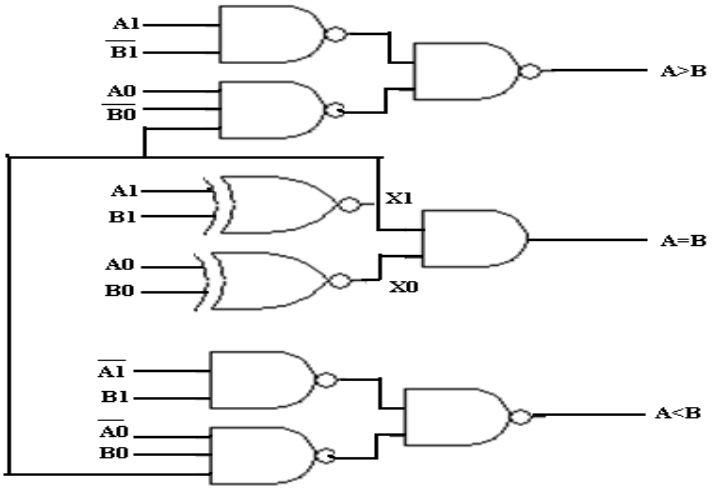



**Figure 2. Logic Diagram of 2-Bit Magnitude Comparator**

## 3. 2-BIT MAGNITUDE COMPARATOR DESIGN USING DIFFERENT LOGIC STYLES

### 3.1. Using CMOS Logic Style

Fig.3 (a) represents symbol of CMOS Inverter. It consists of one NMOS & one PMOS transistor. If input A=0 (logic low) then both gates are at zero potential & PMOS is ON & provide low impedance path from $V_{DD}$ to output (Y). Therefore output (Y) approaches to high level of $V_{DD}$. If input A=1 (logic high) then both gates are at higher potential but NMOS is ON & provide low impedance path between ground & output (Y). Therefore, output (Y) approaches to low level of 0V [1]. The substrate for the NMOS is always connected to ground, while the substrate for the PMOS is always connected to $V_{DD}$, so it is ignored in the diagrams for simplicity.

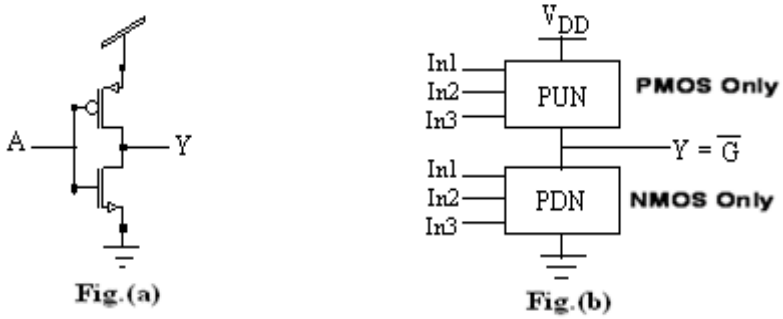



**Figure 3. (a) Symbol of CMOS Inverter (b) Logic Network of CMOS Style**

CMOS logic style is really extension of CMOS inverters to multiple inputs [6]. Logic network of CMOS style is shown in Fig.3 (b). The principle of CMOS logic design says that Pull up network has only PMOS circuitry & Pull down network has only NMOS circuitry. The function of PUN is to provide connection between output & $V_{DD}$, similarly of PDN is to provide connection between output & GND. PUN and PDN networks are constructed in a fashion such that one & only one network is conducting at a time [7]. Number of transistors for N-input logic gate is 2N. Any logic function can be realized by NMOS pull-down and PMOS pull-up networks connected between the gate output and the power lines. Schematic of 2-bit magnitude comparator using CMOS logic style is given in Fig.4.

**Advantages**

- Design provides full output voltage swing between 0 and $V_{DD}$.
- It provides high noise immunity because it has low sensitivity to noise.
- Provides high noise margin because $V_{OH}$ & $V_{OL}$ are nearly at $V_{DD}$ & GND, respectively.
- It is called Ratioless logic due to balanced device [8].

**Disadvantages**

- Design produces Large Power dissipation in comparison to remaining three logic styles.
- Design requires large number of transistors because for every input both (NMOS & PMOS) are used.

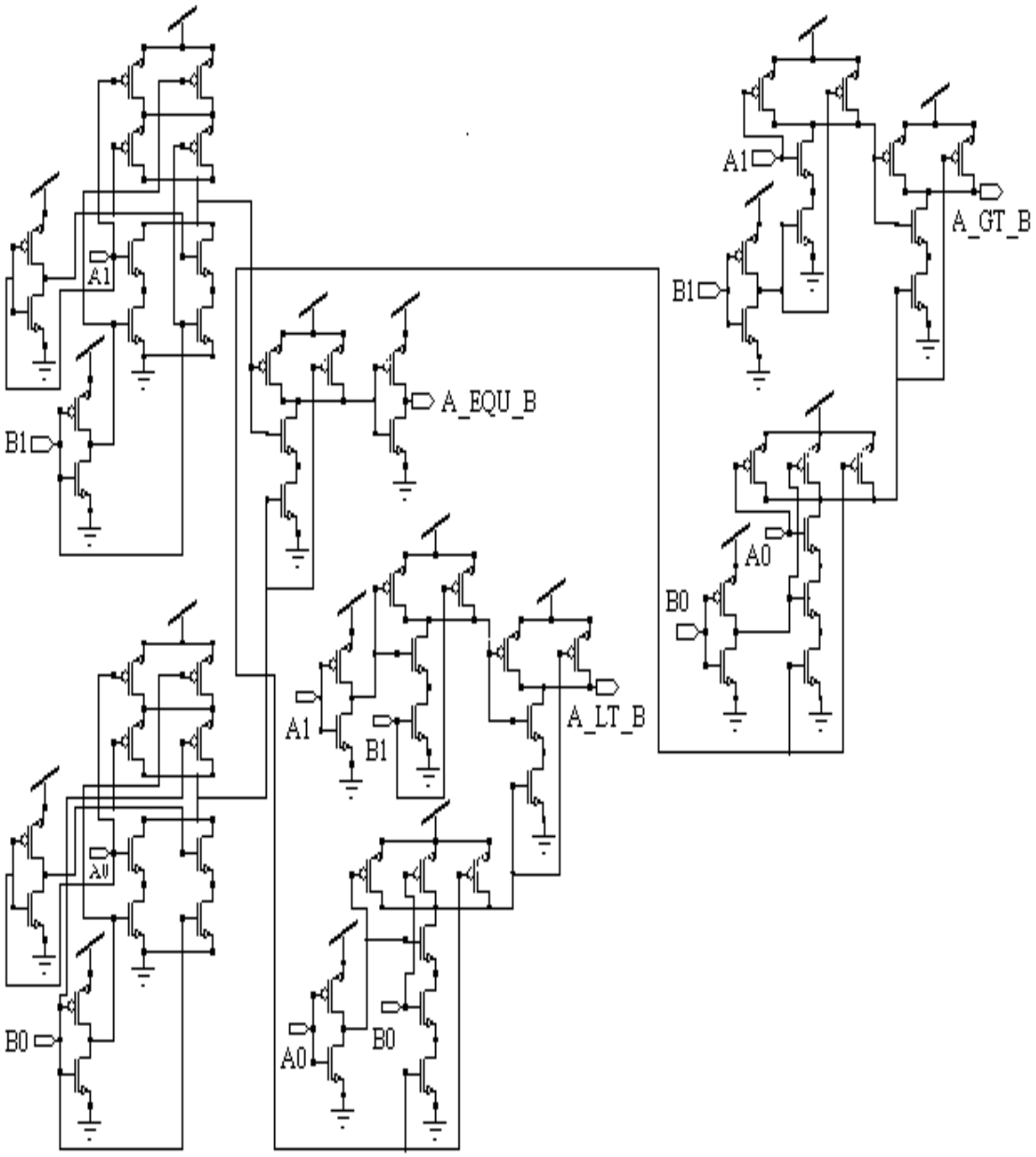



**Figure 4. Schematic of 2-Bit Magnitude Comparator using CMOS logic style**

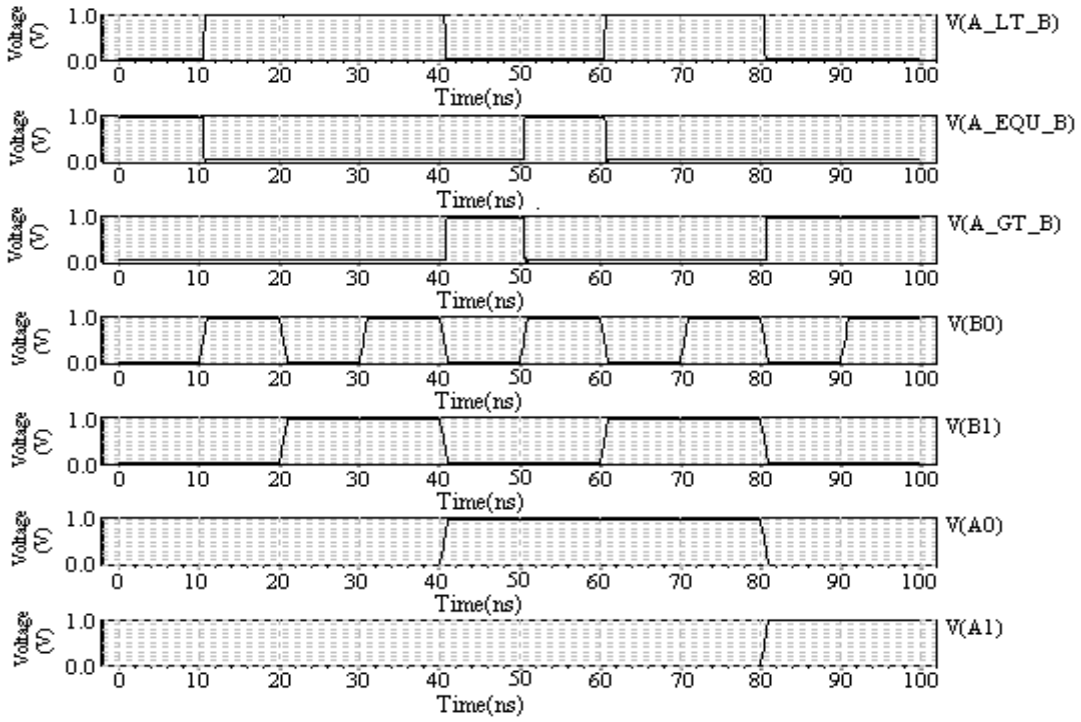



**Figure 5. Waveform of 2-Bit Magnitude Comparator using CMOS logic style**

Consider input bits 0100 then according to truth table in output side, '1' should be obtained in A>B & rest two output should be '0'. After simulation output waveform (in Fig.5) shows same result as in truth table for these input bits. When input bits are 0101 then expected output in A=B should be '1', & waveform also shows same output as in truth table. Similarly, When input bits are 0110 then expected output in A<B should be '1', & waveform also shows same output as in truth table.
After simulation, for CMOS design style, results at different voltages are obtained and given in Table 2.

**Table 2. Simulation results for 2-Bit Magnitude Comparator using CMOS style**

| Input Voltage and Supply Voltage (volts) | Power Consumption (watts) | Delay Time (seconds) | Power-Delay Product (ws) |
|---|---|---|---|
| 0.6 | 5.3343e-009 | 3.0386e-008 | 16.2088e-017 |
| 0.8 | 8.6669e-009 | 3.0321e-008 | 26.2789e-017 |
| 1.0 | 1.4058e-008 | 3.0234e-008 | 4.2502e-016 |
| 1.2 | 2.1032e-008 | 2.9963e-008 | 6.3018e-016 |
| 1.4 | 2.8080e-008 | 2.9958e-008 | 8.4122e-016 |

At 0.6v supply voltage, power consumption is 5.3343e-009watts & delay is 3.0386e-008sec. At high supply voltage (1.4v), power consumption is 2.8080e-008watts & delay is 2.9958e-008sec. Means power consumption is increased by increasing supply voltage, which is satisfactory factor since Power Consumption is directly proportional to supply voltage [1] & delay is reduced by increasing supply voltage, which is also satisfactory factor since delay is inversely proportional to supply voltage. Graphs are given in Fig.15, 16 & 17.

### 3.2. Using Transmission Gate (TG) Logic Style

Transmission Gate is also called as Pass Gate [1]. It consists of one NMOS & one PMOS transistor, connected in parallel as in Fig.6. Transmission Gate operates as bidirectional switch between nodes A & Y that is controlled by signal C. If C=1 (logic high) or $\overline{C}$=0, then both transistors are ON & provide low resistance current path between node A & Y. If C=0 (logic low) or $\overline{C}$=1, then both transistors are off & provide open circuit path between node A & Y. This condition is known as high impedance state. If A=0, then signal passes through NMOS because NMOS is strong '0', and If A=1, then signal passes through PMOS because PMOS is strong '1'. Schematic of 2-bit magnitude comparator using transmission gate logic style is given in **Fig.7.**

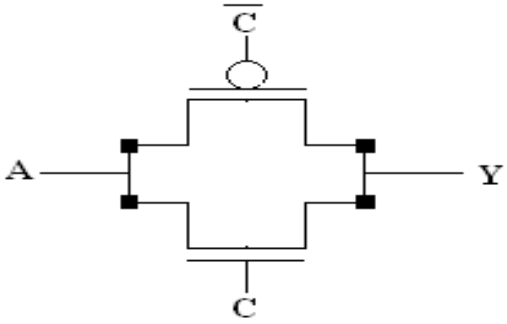



**Figure 6. Symbol of Transmission Gate**

**Advantages**

- It provides full output swing because '1' passes through PMOS & '0' through NMOS.
- It acts as bidirectional switch.
- It produces high noise margin because $V_{OH}$ & $V_{OL}$ are nearly at $V_{DD}$ & GND, respectively.

**Disadvantages**

- Design requires large number of transistors.
- It produces Large Power dissipation than PTL and Pseudo logic styles.
- Design is much complex because Control signal requires both true & complimentary form.

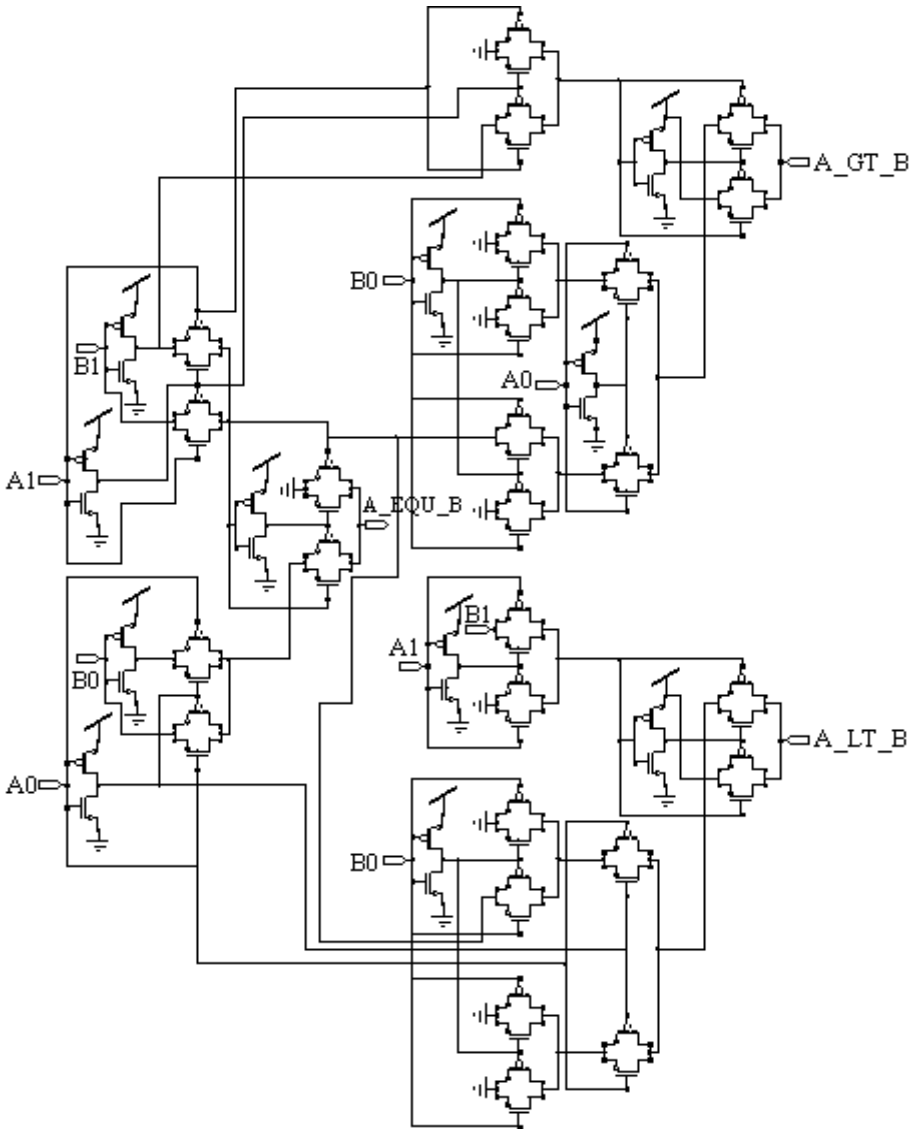



**Figure 7. Schematic of 2-Bit Magnitude Comparator using Transmission Gate logic style**

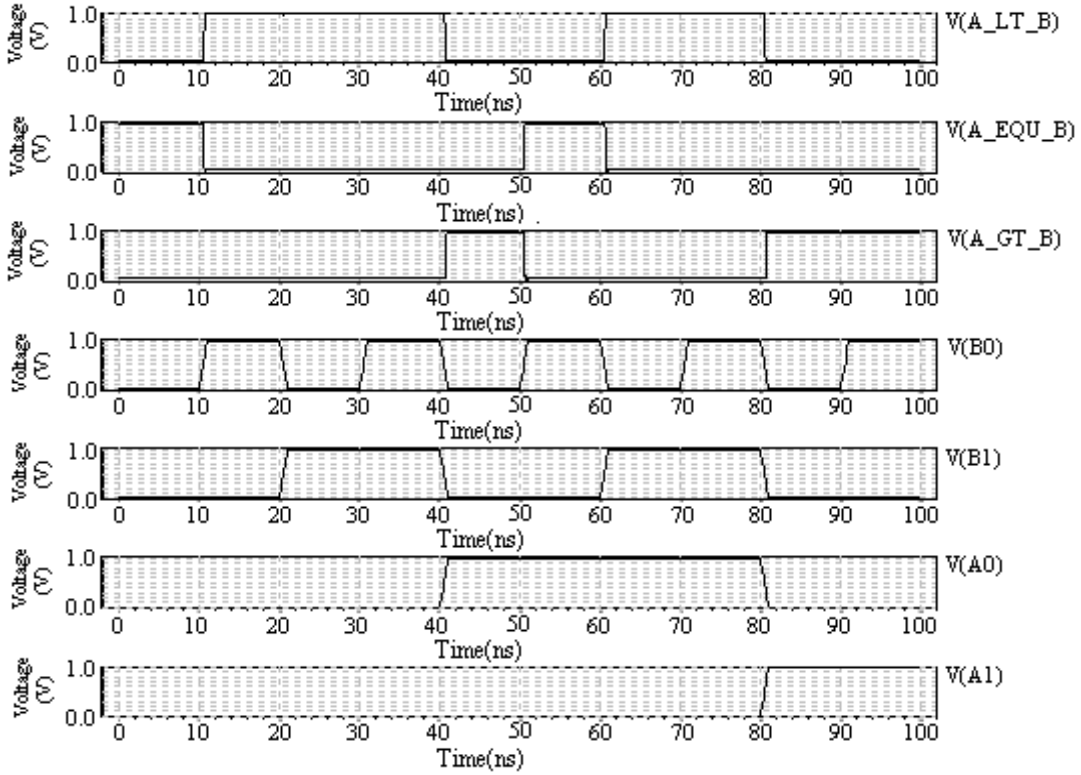



**Figure 8. Waveform of 2-Bit Magnitude Comparator using Transmission Gate logic style**

Consider input bits 0100 then according to truth table in output side '1' should be obtained in A>B & rest two output should be '0'. After simulation output waveform (in Fig.8) shows same result as in truth table for these input bit. When input bits are 0101 then expected output in A=B should be '1', & waveform also shows same output as in truth table. Similarly, When input bits are 0110 then expected output in A<B should be '1', & waveform also shows same output as in truth table.
After simulation, for TG design style, results at different voltages are obtained and given in **Table 3**.

**Table 3. Simulation results for 2-Bit Magnitude Comparator using TG style**

| Input Voltage and Supply Voltage (volts) | Power Consumption (watts) | Delay Time (seconds) | Power-Delay Product (ws) |
|---|---|---|---|
| 0.6 | 4.0802e-009 | 2.9994e-008 | 12.2381e-017 |
| 0.8 | 8.2429e-009 | 2.9988e-008 | 24.7188e-017 |
| 1.0 | 1.3249e-008 | 2.9981e-008 | 3.9721e-016 |
| 1.2 | 1.9855e-008 | 2.8940e-008 | 5.7460e-016 |
| 1.4 | 2.6677e-008 | 2.8085e-008 | 7.4922e-016 |

At 0.6v supply voltage, power consumption is 4.0802e-009watts & delay is 2.9994e-008sec. At high supply voltage (1.4v), power consumption is 2.6677e-008watts & delay is 2.8085e-008sec. Means power consumption is increased by increasing supply voltage, which is satisfactory factor since Power Consumption is directly proportional to supply voltage & delay is reduced by increasing supply voltage, which is also satisfactory factor since delay is inversely proportional to supply voltage. Graphs are given in Fig.15, 16 & 17.

### 3.3. Using Pseudo NMOS Logic Style

In Pseudo NMOS logic style, single PMOS transistor is used in place of Pull-up network as a load with its gate terminal always connected to ground [1] as in Fig.9. In this logic entire PUN is replaced with single load device that pulls up the output [6]. Number of transistors for N-input logic gate is N+1. Pseudo NMOS logic style is used where majority of outputs are high, such as address decoder in memory & where speed is more important. Schematic of 2-bit magnitude comparator using pseudo NMOS logic style is given in **Fig.10**.

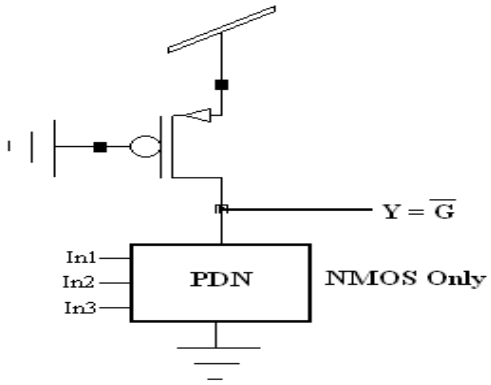



**Figure 9. Logic Network of Pseudo NMOS Style**

**Advantages**

- Design requires less number of transistors than CMOS and TG styles.
- Speed is more because less number of transistors are used in design.
- Logic style reduces dynamic power by reducing capacitive loading.

**Disadvantages**

- It does not provide full output voltage swing because PMOS is always ON by which output resistance is increased then always degraded output is obtained.
- Low noise margin due to high VOL.
- It produces non-zero static power dissipation due to always ON PMOS load device. When NMOS network is turned ON, a direct path between supply voltage and ground exists and then conducts steady state current.

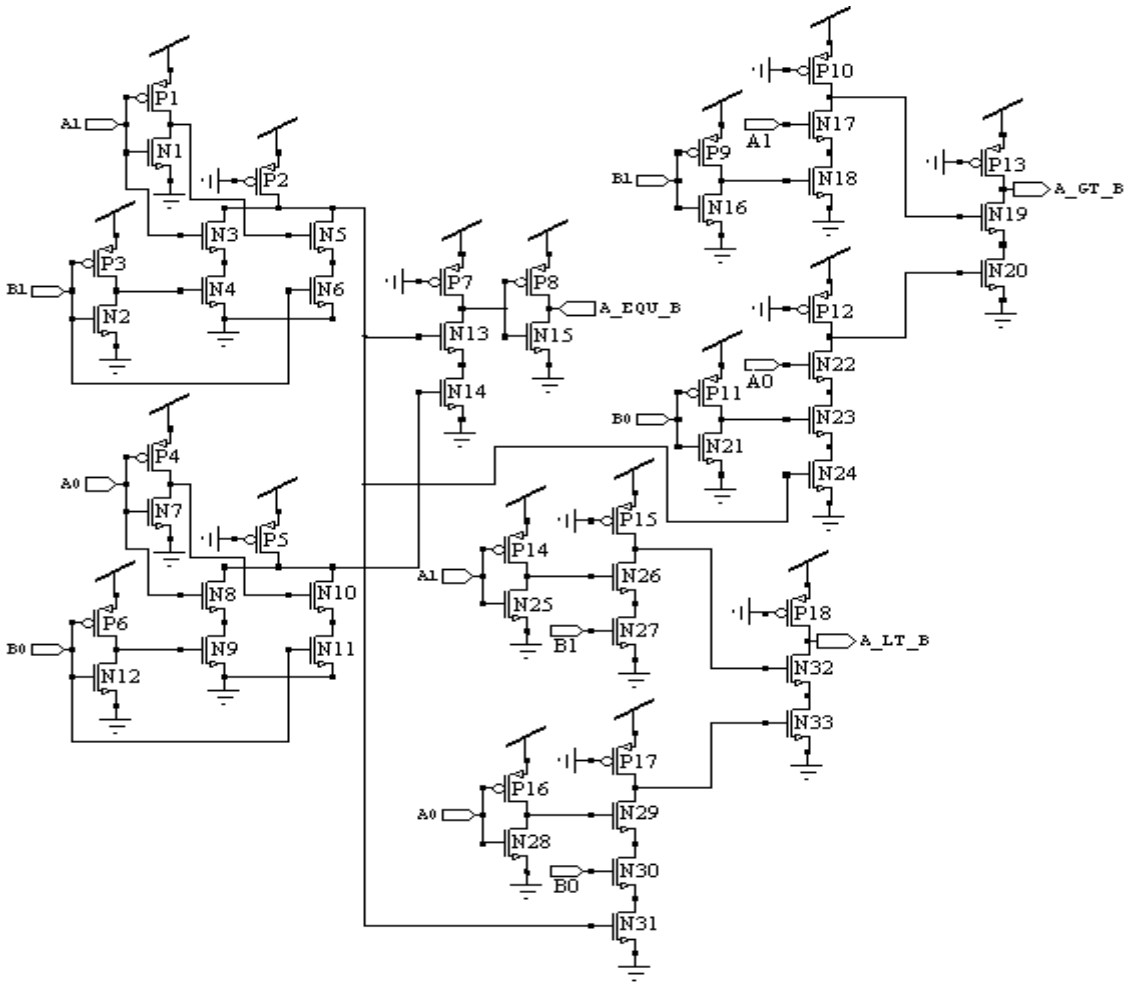



**Figure 10. Schematic of 2-Bit Magnitude Comparator using Pseudo NMOS logic style**

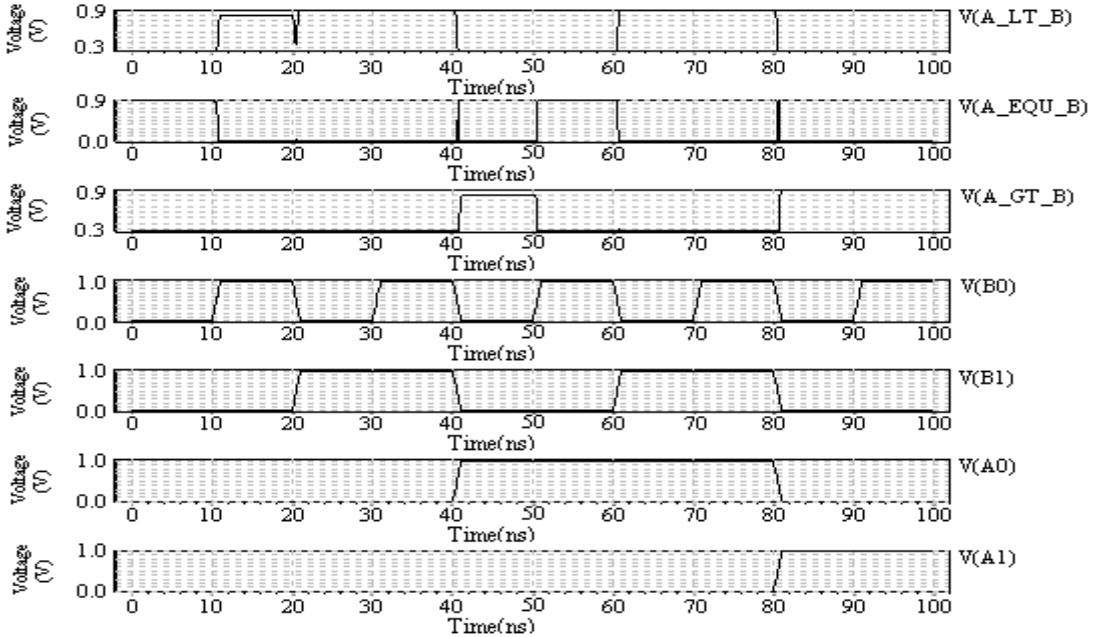



**Figure 11. Waveform of 2-Bit Magnitude Comparator using Pseudo NMOS logic style**

Consider input bits 0100 then according to truth table in output side '1' should be obtained in A>B & rest two output should be '0'. After simulation output waveform (in Fig.11) shows same result as in truth table for these input bit. When input bits are 0101 then expected output in A=B should be '1', & waveform also shows same output as in truth table. Similarly, When input bits are 0110 then expected output in A<B should be '1', & waveform also shows same output as in truth table.

For the input bits 0001, expected output of A<B should be '1'. But here we are seeing that the output A<B is not completely '1'. Means there is a threshold loss there. The reason behind problem is that for these input bits (0001) both the transistors (N32 & P18) are on at the same time then output resistance is increased. That's why degraded output is obtained.

After simulation, for Pseudo design style, results at different voltages are obtained and given in **Table 4**.

**Table 4. Simulation results for 2-Bit Magnitude Comparator using Pseudo NMOS style**

| Input Voltage and Supply Voltage (volts) | Power Consumption (watts) | Delay Time (seconds) | Power-Delay Product (ws) |
|---|---|---|---|
| 0.6 | 2.6661e-009 | 2.9845e-008 | 7.9569e-017 |
| 0.8 | 4.6755e-009 | 2.9775e-008 | 13.9213e-017 |
| 1.0 | 7.2399e-009 | 2.0034e-008 | 21.7443e-017 |
| 1.2 | 1.0353e-008 | 2.0027e-008 | 2.0733e-016 |
| 1.4 | 1.4317e-008 | 2.0019e-008 | 2.8661e-016 |

At 0.6v supply voltage, power consumption is 2.6661e-009watts & delay is 2.9845e-008sec. At high supply voltage (1.4v), power consumption is 1.4317e-008watts & delay is 2.0019e-008sec. Means power consumption is increased by increasing supply voltage, which is satisfactory factor since Power Consumption is directly proportional to supply voltage & delay is reduced by increasing supply voltage, which is also satisfactory factor since delay is inversely proportional to supply voltage. Graphs are given in Fig.15, 16 & 17.

### 3.4. Using Pass Transistor Logic (PTL) Style

Main idea behind PTL is to use purely NMOS Pass Transistors network for logic operation [1]. The basic difference of pass-transistor logic style compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines as in Fig.12. In this design style, transistor acts as switch to pass logic levels from input to output [9]. Schematic of 2-bit magnitude comparator using pass transistor logic style is given in Fig.13.

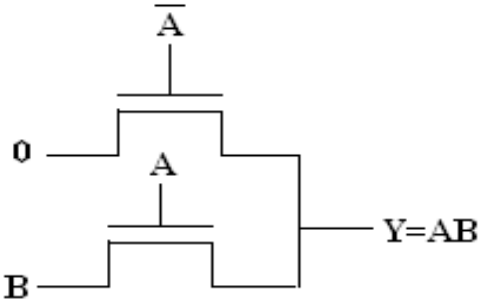



**Figure 12. Symbol for AND Gate using Pass Transistor Logic**

**Advantages**

- Design requires less number of transistors because one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation.
- Speed is increased because less number of transistors are used for design.
- Less area is required for design because PMOS is not used.

**Disadvantages**

- It does not provide full output voltage swing because PMOS is not used.
- Design produces threshold loss because it uses only NMOS transistors to pass both Low & High (‘0’ & ‘1’) inputs.

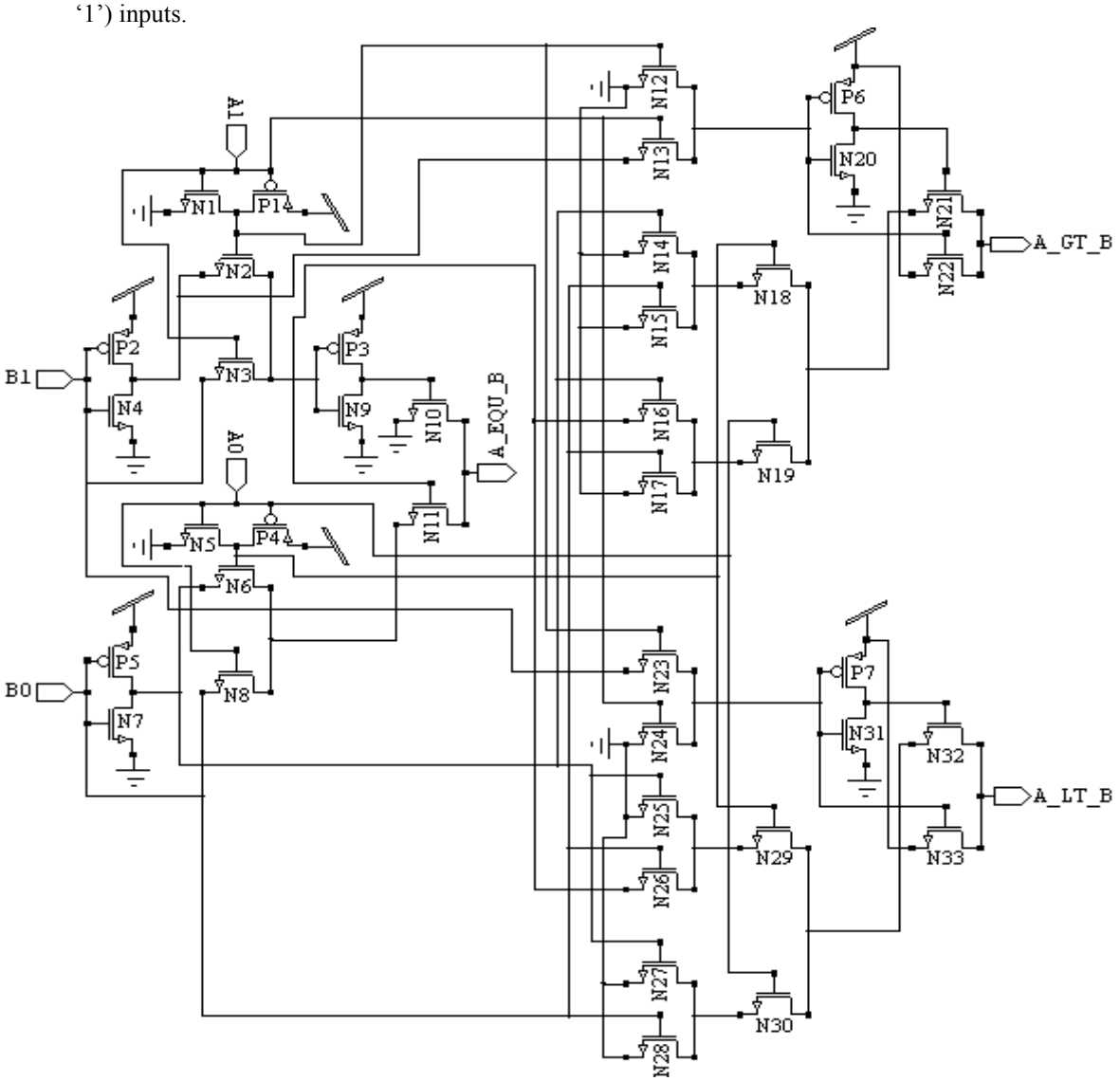



**Figure 13. Schematic of 2-Bit Magnitude Comparator using Pass Transistor Logic style**

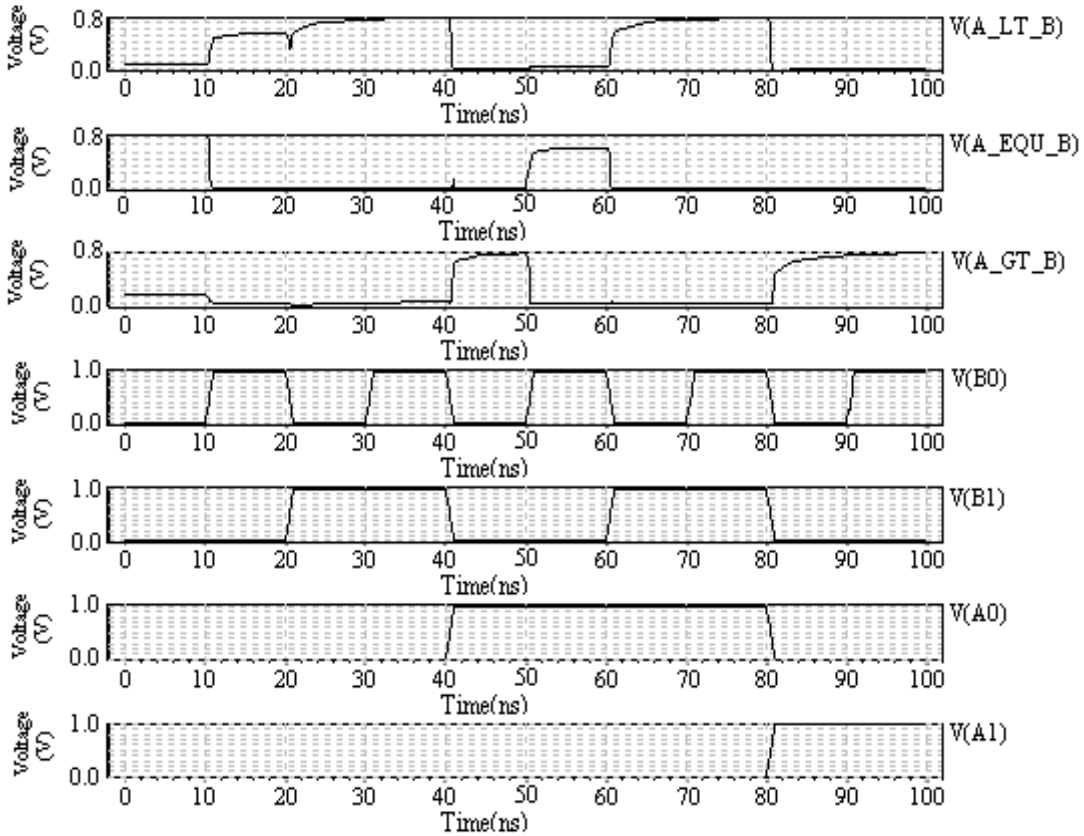



**Figure 14. Waveform of 2-Bit Magnitude Comparator using Pass Transistor Logic style**

Consider input bits 0100 then according to truth table in output side '1' should be obtained in A>B & rest two output should be '0'. After simulation output waveform (in Fig.14) shows same result as in truth table for these input bit. When input bits are 0101 then expected output in A=B should be '1', & waveform also shows same output as in truth table. Similarly, When input bits are 0110 then expected output in A<B should be '1', & waveform also shows same output as in truth table.

For the input bits 0001, expected output of A<B should be '1'. But here we are seeing that the output A<B is not completely '1'. Means there is a threshold loss there. The reason behind problem is that this '1' is passing through NMOS transistors (N26, N29, N32) and we know that NMOS is weak '1' device. That's why these NMOS do not passing here complete '1'. To overcome this problem, we can increase size of these NMOS transistors.

After simulation, for PTL design style, results at different voltages are obtained and given in **Table 5.**

**Table 5. Simulation results for 2-Bit Magnitude Comparator using PTL style**

| Input Voltage and Supply Voltage (volts) | Power Consumption (watts) | Delay Time (seconds) | Power-Delay Product (ws) |
|---|---|---|---|
| 0.6 | 1.7310e-009 | 3.0961e-008 | 5.3593e-017 |
| 0.8 | 3.0350e-009 | 3.0163e-008 | 9.1544e-017 |
| 1.0 | 4.6177e-009 | 3.0135e-008 | 13.9154e-017 |
| 1.2 | 6.8361e-009 | 2.0077e-008 | 13.7248e-017 |
| 1.4 | 8.9325e-009 | 2.0020e-008 | 17.8828e-017 |

At 0.6v supply voltage, power consumption is 1.7310e-009watts & delay is 3.0961e-008sec. At high supply voltage (1.4v), power consumption is 8.9325e-009watts & delay is 2.0020e-008sec. Means power consumption is increased by increasing supply voltage, which is satisfactory factor since Power Consumption is directly proportional to supply voltage & delay is reduced by increasing supply voltage, which is also satisfactory factor since delay is inversely proportional to supply voltage. Graphs are given in Fig.15, 16 & 17.

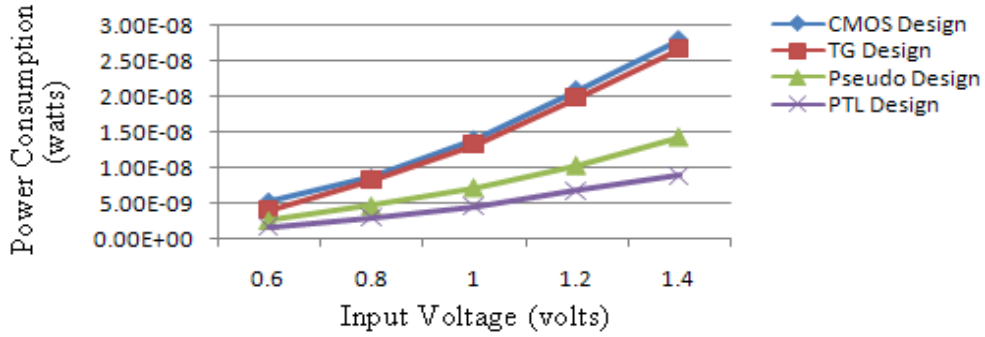



**Figure 15. Power Consumption vs Input Voltage**

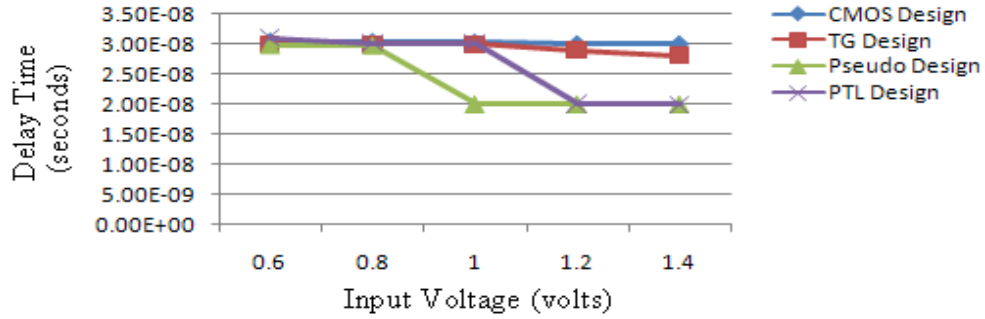



**Figure 16. Delay Time vs Input Voltage**

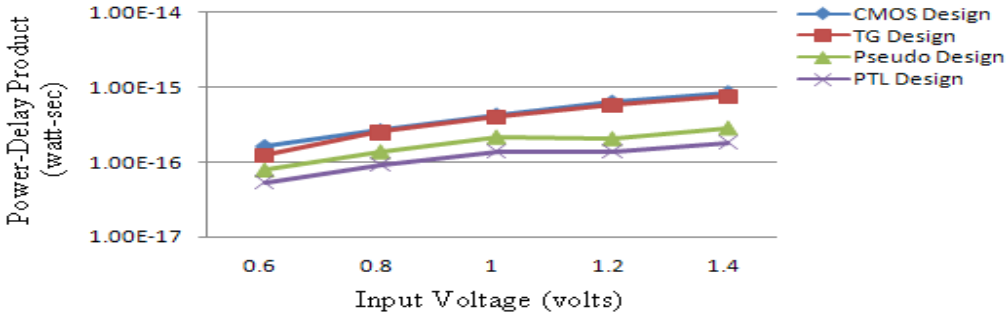



**Figure 17. Power-Delay Product vs Input Voltage**

## 4. CONCLUSION

After simulation of all four designs final results are obtained for Power Consumption, Delay, Power Delay Product. PTL Logic Style provides low power design as compared to other Logic Style. Pseudo NMOS logic style provides less delay as compared to other logic style. PTL Logic Style provides less PDP as compared to other logic style. It has been found that transistor count is less in PTL style design than that of other logic style design. An important factor, output voltage swing is better in CMOS logic style design & Transmission Gate design. But Transmission Gate logic style requires transistor count more than CMOS design style. Pseudo NMOS logic style and PTL style do not provide full output voltage swing.

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