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Optimal design of a Wide Range Pre-charging Three Stage Ring Voltage Control Oscillator at 32nm technology

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Abstract: *The current starved ring vco requires 5 minimum stages to get the optimum oscillations. But the differential ring vco attains the required oscillations within three stages only. It maintains the minimal power dissipation even after the allocation of three vco stages and hence mostly preferred for RF applications. The conventional ring VCO has limitation of low tuning range. So overcome this limitation, a pre-charge P-channel MOSFET is added to the design. After the addition of this efficient component to the ring VCO design, VCO oscillation frequency rise to 10.1-13.97 GHz with tuning voltage of 0-3.4V. The phase noise obtained from this ring VCO is -97 dBc/Hz at 1MHz offset frequency and FOM is -179.47 dBc/Hz. It is an efficient implementation as compared to the peer ring VCO designs as depicted in the research paper. The circuit is designed to operate at 1.2V supply supplemented with power consumption of 0.566-0.951 mW.*

Keywords*: Voltage Controlled Oscillator, PhaseNoise, Low Power, Pre-charge, Ring, Tuning Voltage*

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I. Introduction

Voltage Controlled Oscillators (VCO) is complemented with wide range of applications, especially in the RF domain. Phase Lock Loop (PLL) design, which is one of the important application of VCO, incorporates VCO at its last stage of generation of the output. The phase locking is depended on this component. Federal Communication Commission (FCC) has regulated the use of 3.1-10 GHz frequency range for commercial use. For this, low cost systems with manageable complexity is required, e.g. Wireless Sensor Network(WSN), Radio Frequency ID(RFID) or Wireless Body Area Network(WBAN) [1]. This in turn necessitates the use of a precise VCO, viz. Ring VCO. LC VCO may not be a preferred choice for this application because of its prevalent complexity as well as relatively higher cost and large area requirement because of the inculcation of inductor.

The conventional ring VCO has fewer associated problems such less tuning range & high phase noise. This research contribution appends pre-charged PMOS to the ring oscillator architecture to help resolve the problem of phase noise and frequency range.

Section II elaborates the ring VCO design. Section III describes the design of a three stage ring VCO. Section IV exemplifies the results obtained from the three stage ring VCO and establishes a comparative study with the peer ring VCO architectures. Section V concludes the paper.

II. Ring VCO

The Proposed circuit of a ring VCO is shown in Fig.1. It consists of M1 and M2 NMOS which forms differential input block. They are clubbed together with M3 and M4 to form a CMOS latch, which strengths oscillation frequency. M5 and M6 acts as controlling block, used to control the CMOS latch block and are responsible for generating variable frequency on the basis of control voltage applied at the inputs of M5 and M6. M7 and M8 are used to reduce phase noise and speedup the oscillation frequency. M9 and M10 are the pre-charging devices which are added to the acceleration block to reduce the rise time as well as fall time and helps to pre-charge the output. So overall combination of these devices are used to increase the frequency range as compared to the conventional architecture [2].

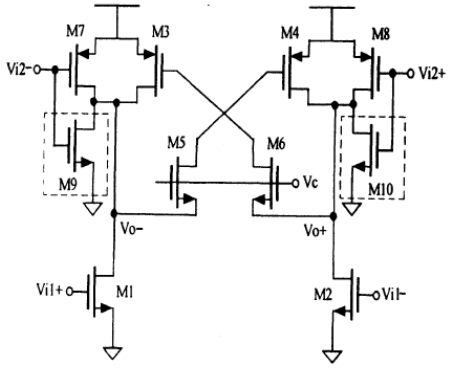

Fig.1 Delay cell with pre-charge MOSFET[2]

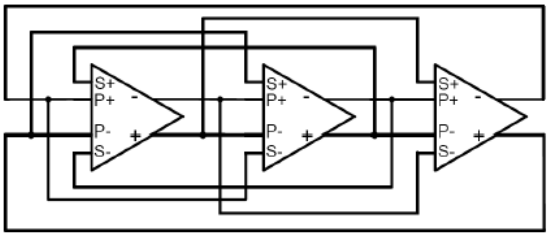

Fig.2 Three stage ring VCO[3]

Fig.2 shows the connection of three stage ring VCO which consists of ten transistors in each delay cell. Each delay cell has a delay of 10ps with center frequency of 10GHz. Transistor sizing was done by using eq.(1)-eq.(5) [4].

$$f = \frac{1}{2Ntdelay} \dots\dots\dots (1)$$

$$tdelay = Reff * Ceff \dots\dots (2)$$

$$Reff = \frac{Vloadmax}{Iloadmax} \dots\dots (3)$$

$$f = \frac{\beta * (Vc - Vt)2}{2NCeffVc} \dots\dots (4)$$

$$Ceff = 0.7 * Cox * (Wswitch * Lswitch + Wload * Lload) \dots\dots (5)$$

Where N is the number of stages, t_{delay} is delay time, f is the frequency, R_{eff} is the effective resistance, C_{eff} is the effective capacitance, $V_{loadmax}$ is maximum load voltage, $I_{loadmax}$ is the maximum load current, β is the process parameter,Vc is the control voltage,Vt is the threshold voltage, Cox is the oxide capacitance, Wswitch and Wload is the width of switch (NMOS) and width of load (PMOS).

Calculations are performed to obtain required oscillation frequency. Width of 120nm and length of 30 nm is kept for all the MOSFETs except controlling block devices. The width and length of controlling block devices are kept at 30nm.

The phase noise and figure of merit is calculated from eq.(5), eq.(6) [5].

$$Lmin(\Delta f) = 10 \log\left(\frac{7.33kTfo2}{Pmin(\Delta f)2}\right) \dots\dots (5)$$

$$FOM = Lmin(\Delta f) - 20 \log\left(\frac{fo}{\Delta f}\right) + 10 \log\left(\frac{Pmin}{1mW}\right) \dots\dots (6)$$

Where Lmin(Δf) is the phase noise at offset frequency, Δf, k is the Boltzmann constant, T is the temperature in K, fo is the oscillation frequency, Pmin is minimum power dissipation, FOM is Figure of Merit.

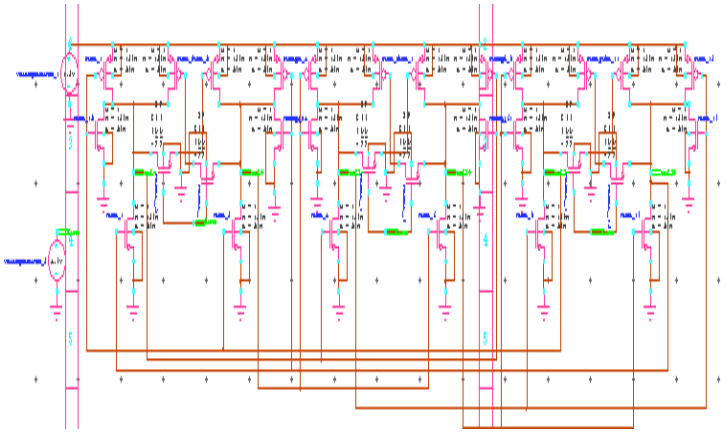

Fig.3 Circuit schematic of a 3-stage Ring VCO using Tanner EDA tool

With help of TANNER EDA tool targeted at 32nm technology, three stage saturated ring VCO (Fig. 3) has been designed. Tuning voltage is connected at the controlled block which varies from 0.1-3.4 V and supply of 1.2 V is connected at the source PMOS loads. With this circuit connection, frequency tuning range of 3.87 GHz is achieved i.e. this VCO generates frequency from 10.1-13.97 GHz.

III. Results

3.1. Phase Noise & FOM

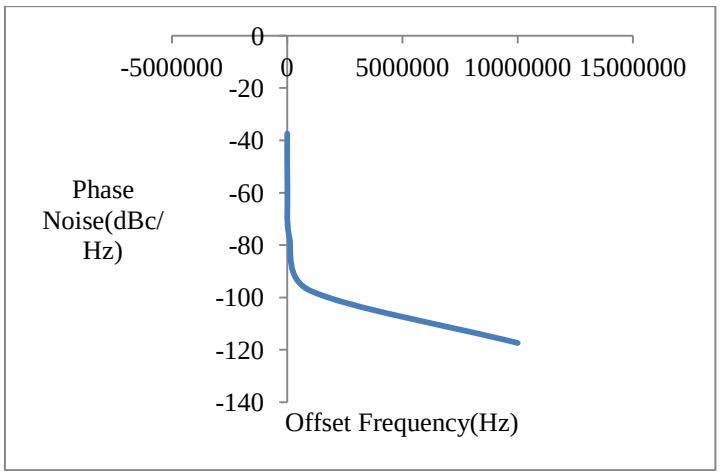

Fig.5 Phase noise vs. Offset frequency graph

The proposed 3 stage Ring VCO design achieves a Phase noise of -97 dBc/Hz (Fig.5) at 1 MHz offset frequency and -117 dBc/Hz at 10 MHz offset frequency. The FOM obtained at 1 MHz offset frequency and power consumption of 0.566 mW is -179.47 dBc/Hz .

3.2. Tuning Voltage vs Frequency graph

As the tuning voltage vary from 0-3.4 V, the frequency range of 10.1 GHz-13.97 GHz is achieved with central oscillation frequency of 10GHz, which is a huge gain in the frequency as compared to the previous designs. Fig. 7(a) shows oscillation frequency at Vtune = 0 V producing 10.1GHz and Fig. 7 (b) oscillation at Vtune = 3.4 V producing 13.97GHz.

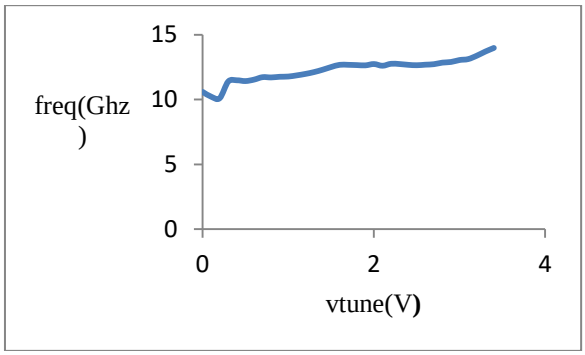

Fig.6. Tuning voltage vs. Frequency graph

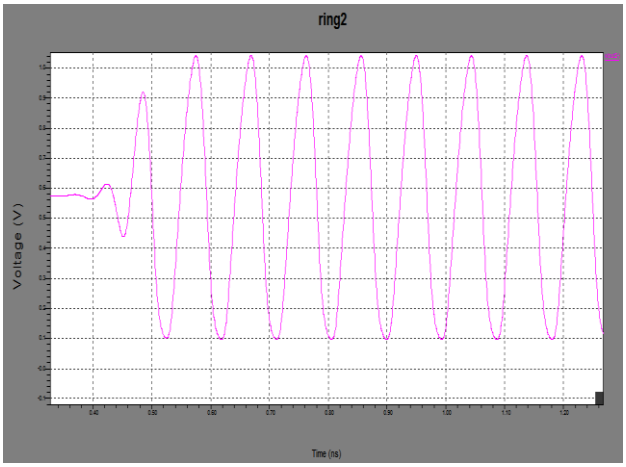

Fig.7(a) Oscillation at Vtune = 0V

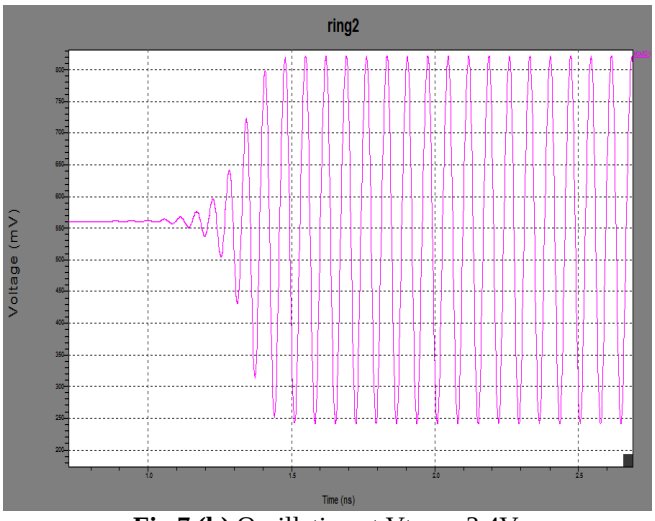

Fig.7 (b) Oscillation at Vtune=3.4V

3.3. TUNING RANGE

The tuning range obtain by

$$tuning\ range = \frac{fmax - fmin}{fosc} * 100$$

Where *fmax* is maximum frequency, *fmin* is minimum frequency and *fosc* is oscillation frequency. The tuning range of 38.7% is obtain by putting *fmax* = 13.97 GHz, *fmin* = 10.1 GHz and *fosc* = 10 GHz.

3.4. COMPARATIVE STUDY OF RESULTS

Reference	Tuning Range(GHz)	Power (mW)	Phase Noise (dBc/Hz)	FOM (dBc/Hz)
Proposed work	10.1-13.97	0.566-0.951	-97	-179
[1]	2.5-7	2.2	-89.2	-160
[7]	10.6-8.4	52.5	-85	-147
[2]	0.85-2.1	10.2	-	-
[8]	0.075-6.9	9.3	-85	-
[3]	4-12.5	3.4-8	-82	-153
[9]	3.2-10	15	-90	-154

IV. Conclusion

The design of a wide range low phase noise Ring VCO is illustrated at 32nm technology. It has been concluded from comparative table that at sub-micron technology, the pre-charging devices has provided wide range as well as phase noise and figure of merit is better as compared to the other ring VCOs. The proposed 3 stage ring VCO design is characterized by low power operation at 0.566-0.951 mW with a minimal supply voltage of 1.2 V. Phase noise of -97 dBc/Hz and FOM of -179.47 dBc/Hz is obtained using pre-charge ring VCO architecture with tuning range of 3.87 GHz.

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