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Performance Investigation of Dmcg-Hcptfet

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Abstract : *The Tunnel Field-Effect Transistor (TFET) Based On Charge Plasma Concept Efficiently Replaces The Conventional TFET As It Offers Fabrication Simplicity And It Can Be Used For Ultra-Low-Power Applications. Charge Plasma TFET (CPTFET) With Hetero Materials Is Developed For The Enhancement Of Device Performance. For This, Instead Of Silicon In Source Region A Narrow Band Gap Material (Inas) Is Used For Reducing The Lateral Tunneling Distance At The Source/Channel Interface. The Reduced Tunneling Width At The Source/ Channel Junction Enables Higher Band-To-Band Tunneling Generation Rate, Thus The Device Offers Higher ON-State Current. To Further Improve ON-State Current A Dual Material Control Gate Hetero Junction-Charge-Plasma-Based Tunnel FET (DMCG-HCPTFET) Is Presented For The First Time. In This Context, A Comparative Study Of CPTFET And Hetero Junction Charge Plasma TFET (H-CPTFET) Has Been Performed In Terms Of Transfer Characteristic (Ids–Vgs) And Transconductance (Gm).*

Keywords *- TFET-Tunnel Field Effect Transistor, CPTFET-Charge Plasma TFET, DMCG-Dual Material Controlled Gate, HCPTFET-Hetero-Material Based CPTFET, GIDL-Gate Induced Drain Leakage.*

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I. INTRODUCTION

The Enhancement In The Performance Of The MOS Technology Can Be Attributed To The Scaling Of Device Dimensions. When You Make Circuits Smaller, Their Capacitance Reduces, Thereby Increasing Operating Speed And Smaller Circuits Allow More Of Them In The Same Wafer, Dividing The Total Cost Of A Single Wafer Among More Dies. Hence Scaling Significantly Increases Speed, Functionality, Packing Density, Reduces Chip Cost, And So On And Significantly Reduces Power Dissipation [4]–[6].

An Important Concern Raised Is That An Increase In The Passive Power Density For Current MOSFET Technology Is Unavoidable With Continued Scaling. With Decreasing Critical Dimensions And Increasing Device Density, New Design Challenges Are Continually Addressed To Meet The Demand In A Growing Market For Electronics. However, With Great Reduction Come Great Problems, In This Case In The Form Of Unwanted Side Effects, The So Called Short-Channel Effects Which Impacts Performance, Modeling And Reliability. When A MOSFET Is Scaled Down To A Channel Length Of 50nm And Below, GIDL Becomes Very Difficult To Manage And Limits The Ability To Scale Down Transistors For Modern Technology.

TUNNEL Field-Effect Transistors (TFET) Are Attracting Attention Because Of Their Low Sub Threshold Swing And Low OFF-State Leakage Current [4]–[6],[10]. Since The Channel Current Is Controlled By The Tunneling Mechanism On The Source Side, Tfets Are More Immune To Short-Channel Effects Unlike The Conventional Nano Scale Mosfets [7]. However, The Low ON-State Current In Si Tfets, Due To Poor Band-To-Band Tunneling Efficiency, Is A Major Challenge To Be Overcome. This Problem Is Being Extensively Studied Using Strain, Hetero-Structures, Low Band Gap Materials, High-K Gate Insulators [1]-[3], [7].The Charge Plasma-Based Tunnel Field-

Effect Transistor (TFET) Has Been Seen As The Potential Candidate To Replace The Conventional TFET As It Offers Fabrication Simplicity And Its Proficiency To Be Used For Ultra-Low-Power Applications[3]

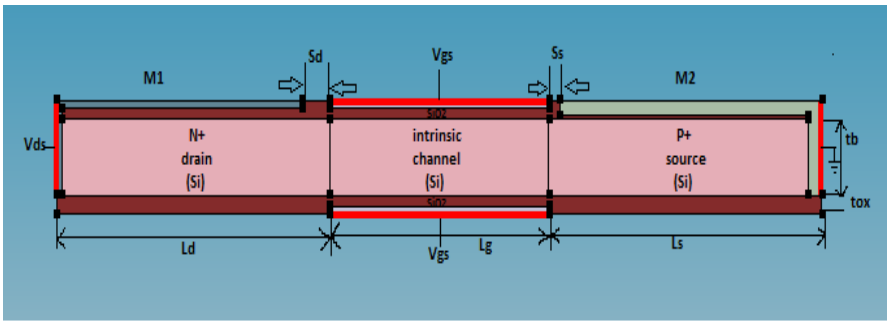
The Idea Of Using Dual Material Gate In The Proposed Device At The Gate Electrode Results In An Improved Device Characteristics. In This Device, Gate Is Divided Into Three Segments, Namely, Tunneling Gate (M1), Control Gate (M2), And Auxiliary Gate (M3), Where Their Corresponding Work Functions Are Φ1, Φ2, And Φ3, Respectively. In Dual Material Control Gate CP-Based TFET (DMCG-CPTFET), $\Phi1 = \Phi3 < \Phi2$ Is Considered, Where Lower Work-Function Φ1 Is Used At Source Side To Improve The BTBT Rate At The Source/Channel Interface, Which Results In An Improved ON-State Current. However, The Fabrication Steps Of DMCG-CPTFET Are Similar To Conventional CP-Based TFET Except The Dual Work-Function Concept In Gate Region Is Used[1].

Since A Charge Plasma P-N Junction Has Already Been Experimentally Demonstrated [12] , The Charge Plasma Based Doping-Less Bipolar Junction Transistor [13], [14] , The Junction-Less TFET Have Been Reported [15] And The Idea Of Dual Material Control Gate CP-Based TFET (DMCG-CPTFET), Which Results In An Improved ON-State Current Is Presented In [1], We Believe That Our Results May Provide The Incentive For Further Exploration Of The DMCG-HCPTFET.

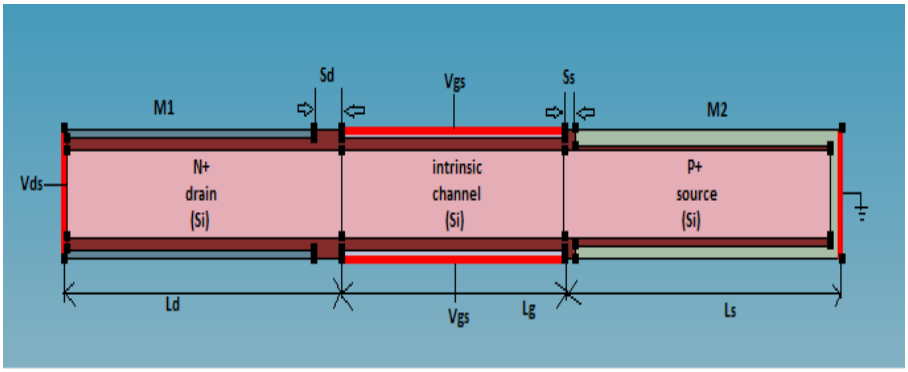
II. DEVICE STRUCTURE AND SIMULATION PARAMETERS

Fig1.A And Fig2.B Shows The Cross-Sectional View Of Different Types Of CPTFET And HCPTFET Respectively. The Design Parameters Of The Devices Used In Simulation Are Reported In Table. In DMCG-CPTFET/HCPTFET, P+ And N+ Regions Are Induced In The Source And Drain Regions, Respectively, Using The CP Concept And Gate Is Divided Into Three Sections With Different Work Function(φ) Values. It Can Be Noticed That OFF Current Reduces As Φ2(Work Function Of M2) Increases. It Happens Due To Wider Tunneling Width. On The Other Hand, OFF Current Starts Increasing (While Keeping ON Current Approximately The Same) On Further Increment In Φ2 > 4.6 Ev Due To The Occurrence Of Band Overlapping Over The Drain Region And Narrower Of Tunneling Barrier Width On Drain Side[4]. Fig Shows The Output Characteristics Of The Proposed Device At Different Vgs Values. It Can Be Inferred That The Drain Current Increases As A Function Of Drain Bias In Triode Region. However, There Is No Remarkable Change In Tunneling Width With Change In Drain Bias Under Saturation Region Owing To The Same Current Throughout This Region. Therefore, We Have Considered Vds = 1 V In The Simulation Where Drain Biasing Is Required. In The Proposed Device, The Aluminum (Φal = 4.08 Ev) And Platinum (Φpt = 5.93 Ev) Are Used To Accomplish The Fundamental Requirement Of CP Concept. However, The Thickness Is Mentioned In TABLE I DESIGN PARAMETERS USED IN SIMULATION OF THE DEVICE. In The Simulation, The Nonlocal BTBT Model Is Incorporated. Shockley Read Hall And Auger Recombination Models Mentioned In [1]–[3] Are Also Included In The Simulation To Incorporate Minority Recombination Effects. We Have Also Used Fermi–Dirac Statistics And Concentration Field-Dependent Mobility Model In The Simulation.

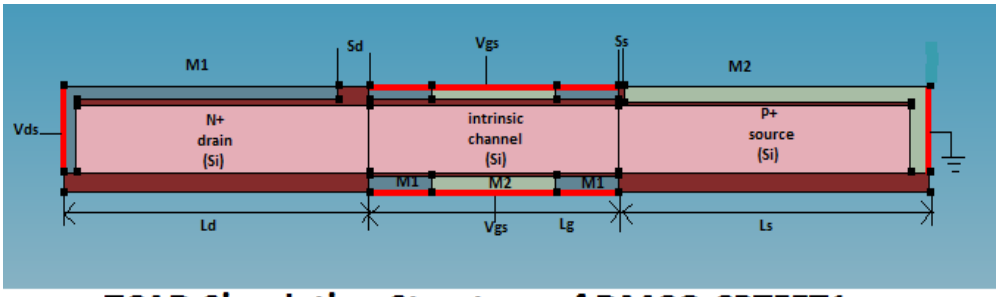
FIGURES AND TABLES



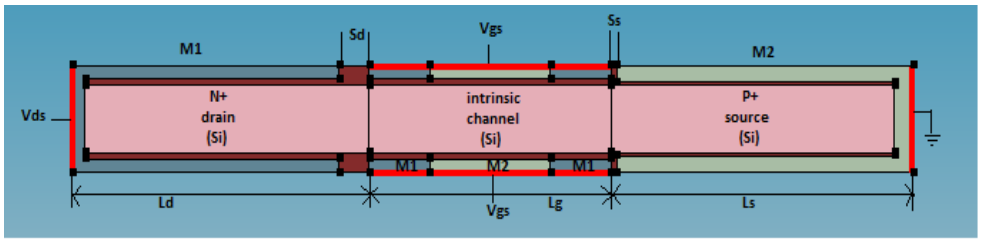
TCAD Simulation Structure of CPTFET1



TCAD Simulation Structure of CPTFET2

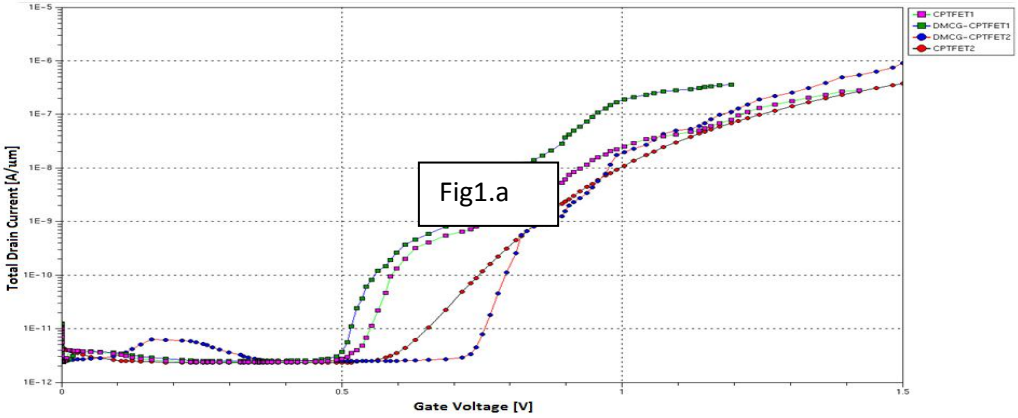


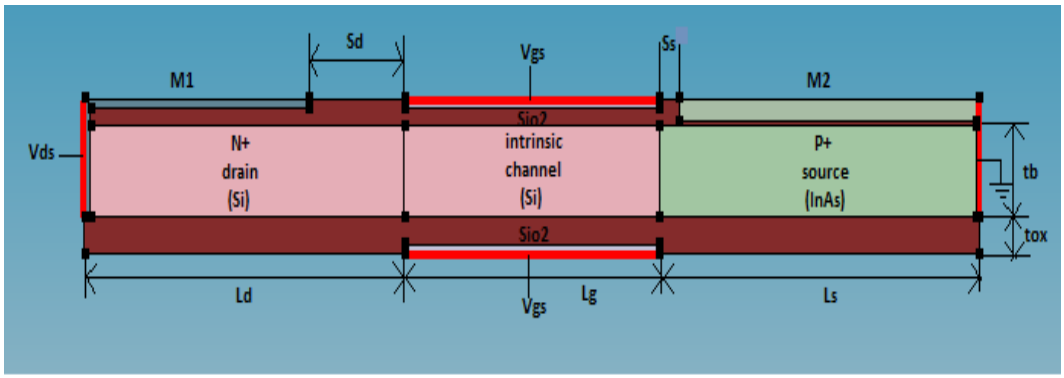
TCAD Simulation Structure of DMCG-CPTFET1



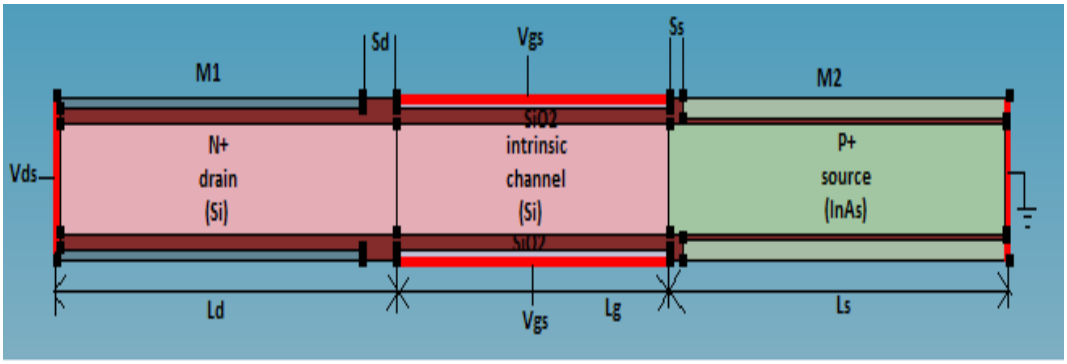
TCAD Simulation Structure of DMCG-CPTFET2

Fig1.b: Ids-Vgs graph

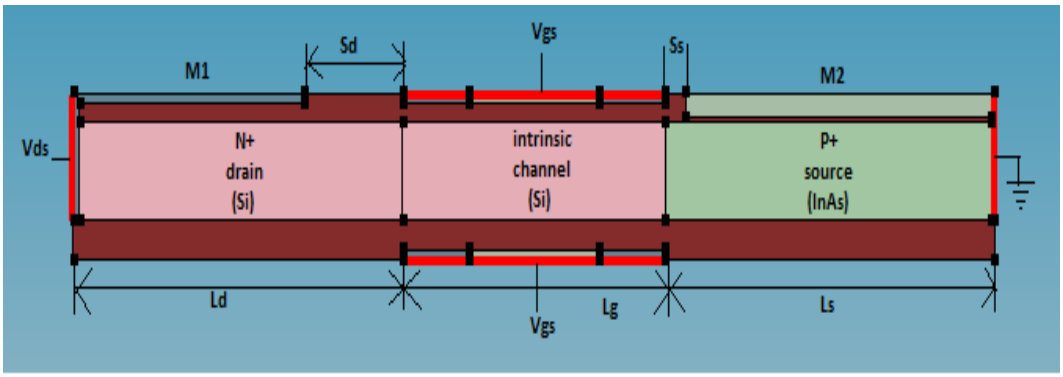




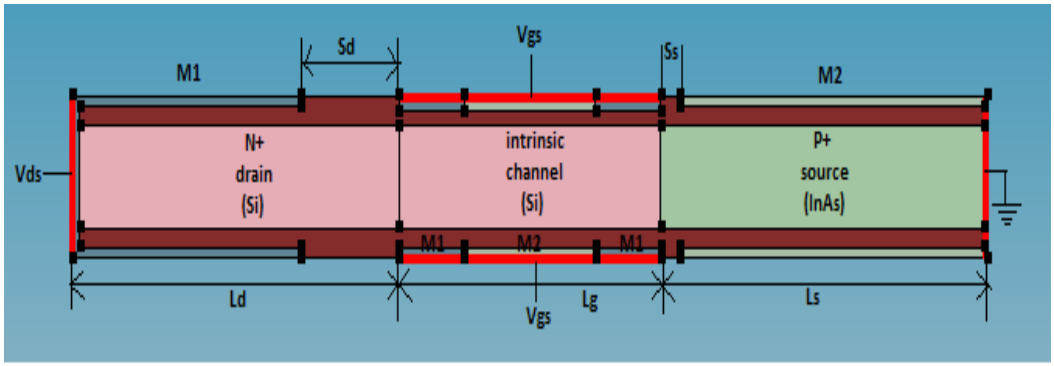
TCAD Simulation Structure of HCPTFET1



TCAD Simulation Structure of HCPTFET2



TCAD Simulation Structure of DMCG-HCPTFET1



TCAD Simulation Structure of DMCG-HCPTFET2

Fig2.a

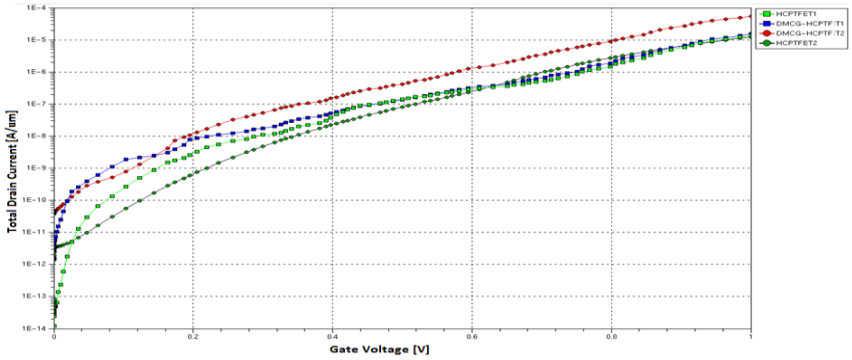


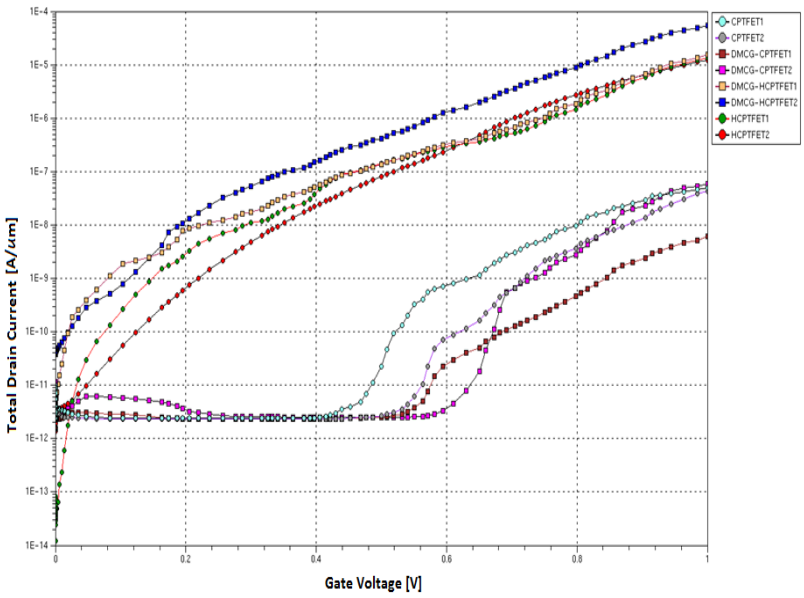
Fig2.b: Ids-Vgs graph

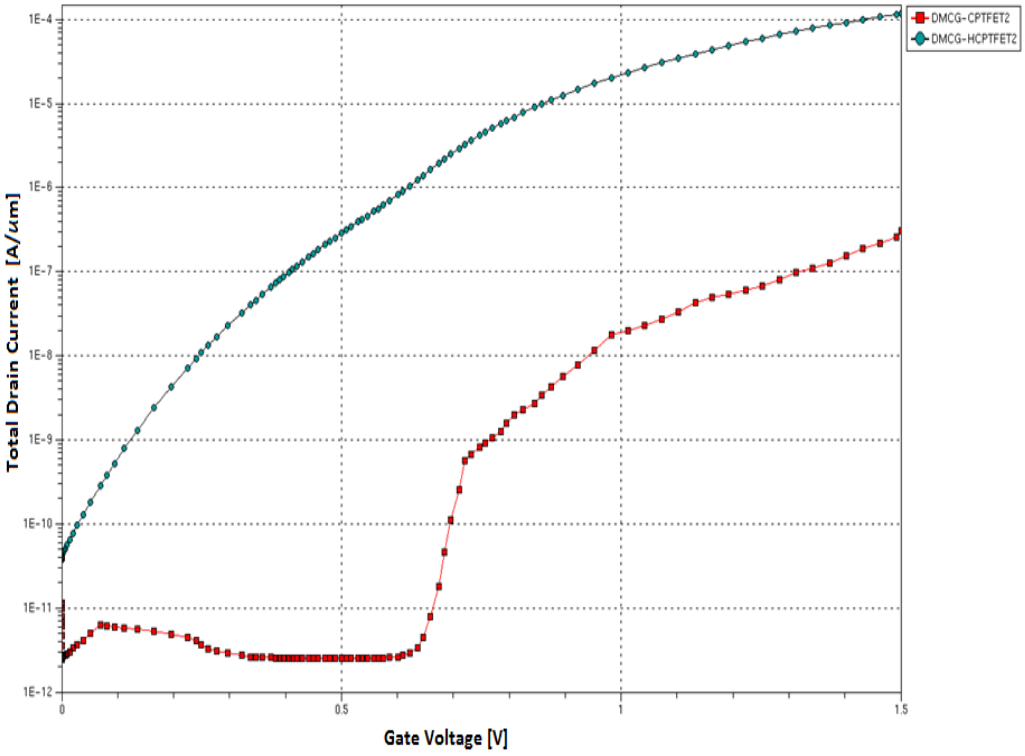
III. RESULTS AND DISCUSSION

Table 1 Physical Parameters Of The Device Used In The Simulation.

Parameters	Values
Channel Length (Lg)	50 Nm
Body Thickness (Tb)	10 Nm
Oxide Thickness (Tox1)	3 Nm
Gate Oxide Material	Sio2
Drain Electrode Work Function (Fm1)	4.08 Ev
Source Electrode Work Function (Fm2)	5.93 Ev
Gate Source Spacing (SS)	3 Nm
Gate Drain Spacing (SD)	15 Nm

In Charge Plasma Concept, The Usage Of Metal Electrodes With Different Work Functions Distributes The Charge Carriers Near To The Surface Depending Upon The Employed Work Function. The Metal Electrode Platinum As A Source Electrode With Oxide Thickness Of 0.5 Nm Maintains The Similar Majority Carrier Concentration In The Source Region, While Minority Carriers Are Distributed Differently For Both OFF And ON State Conditions. On The Other Hand, Aluminum As A Drain Electrode With Oxide Thickness Of 3 Nm Provides Similar Carrier Concentration (Majority And Minority) In Drain/Channel Region. When The Positive Gate Voltage (Vgs) Is Applied, Electron Can Tunnel From Valence Band Of Source Region To Conduction Band Of Channel Region, Hence It Results In Increment Of Carrier Concentration In The Channel Region. In Case Of Hetero-Structure, Since The Source Region Is Made Of Low Band Gap Material, Electrons Can Easily Cross The Tunneling Width When Compared With Conventional CPTFET And On-State Current Is Highly Improved As Observed In Fig1.B And Fig2.B . Hence Hetero-Structures Helps In Reducing The Sub-Threshold Swing As Well [1].





The Presence Of Lower Gate Work Function (Φ1 = 4.08 Ev) In The Case Of DMCG-CPTFET And DMCG-HCPTFET Increases Electron Concentration And Decreases The Hole Concentration Under M1 Section Of Gate With Respect To Single Metal Gate CPTFET And HCPTFET, Whereas The Introduction Of Lower Work-Function At Gate Electrode Toward Drain End For DMCG-HCPTFET And DMCG-CPTFET Increases The Electron Concentration And Decreases The Hole Concentration Under M3 Section Of Gate With Respect To CPTFET And HCPTFET. Sufficient Charge Carriers Are Not Available In The Channel Region At Vgs = 0 And Vds = 1 V, And Thus, All Possible Devices Seem In The OFF-State. The Presence Of Gate Voltage Vgs = 1 V Increases The Electron Concentration And Decreases The Hole Concentration In The ON-State For All Possible Combination Of Devices.

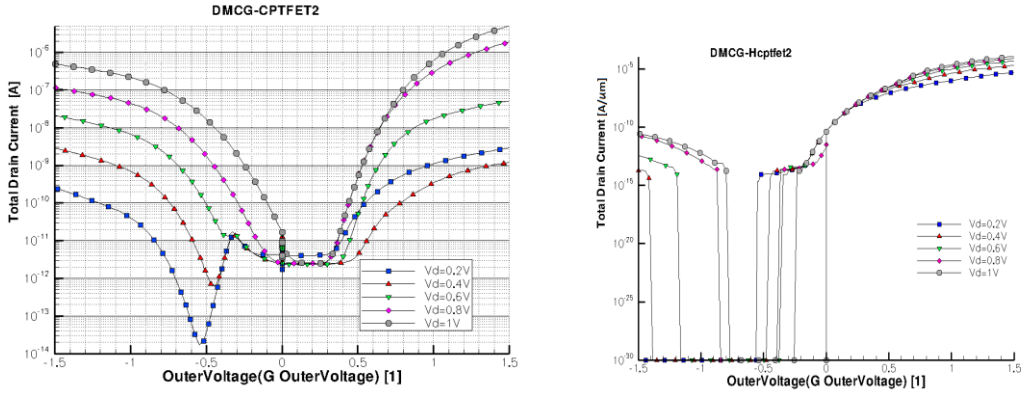


Fig 3: a)Ids-Vgs graph for all CPTFET and HCPTFET
b)Ids-Vgs graph for DMCG-CPTFET2 and DMCG-HCPTFET2

Fig 4. a) Comparative plots of transfer characteristics of DMCG-CPTFET2
b) Comparative plots of transfer characteristics of DMCG-HCPTFET2

From Graphs It Can Be Concluded That Dual Material Controlled Gate Structure Improves On-State Current And As Well As Sub-Threshold Swing. Upon Comparing The Newly Proposed Structure, DMCG-HCPTFET2 With DMCG-CPTFET2 For Ambipolarity In Fig4, It Is Observed That Latter Is Severely Affected From Ambipolar Leakage (Parasitic Conduction) But The Proposed Structure Optimizes The Suppression Of Ambipolar Effects As Well As Transconductance.

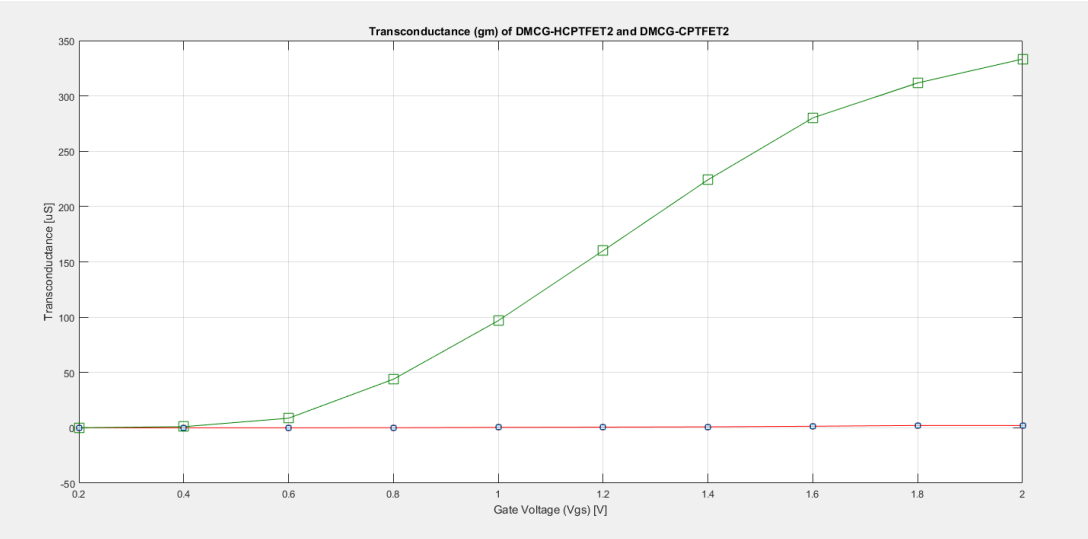


Fig 5: Plot for transconductance of DMCG-CPTFET2 and DMCG-HCPTFET2

Fig. 5 Shows The Transconductance (Gm) Of The Two Devices DMCG-CPTFET2 And Proposed DMCG-HCPTFET2. Transconductance Is The Electrical Characteristic Relating The Current Through The Output Of A Device To The Voltage Across The Input Of A Device Which Basically Shows The Ability Of The Device To Convert Gate Voltage Into Drain Current [11] And Is Formulated As

$$Gm = \frac{\partial Ids}{\partial Vgs} \qquad (1)$$

Drain Current For The Proposed Device DMCG-HCPTFET2 Is Higher Than DMCG-CPTFET2 Due To The Presence Of Hetero Materials In The Device, Wherein The Low Band Gap Material In The Source Region Significantly Reduces The Energy Barrier At The Source/Channel Junction And Enhances The Current Drivability As Shown In Fig3 A And B, Respectively. This Increased Drain Current For DMCG-HCPTFET2 Reflects As Improved Gm For DMCG-HCPTFET2 When Compared With DMCG-CPTFET2 As Depicted In Fig. 5. This Signifies That The Proposed Device Has Better Sensitivity For Converting Gate Voltage Into Drain Current And Provides The Higher Efficiency.

IV. Conclusion

In This Paper, A Comparative Study Of The Different CPTFET And Hetero Charge Plasma TFET (HCPTFET) Is Explored By Using Synopsys Sentaurus TCAD 2014 Version Simulations. It Is Shown That The Usage Of Hetero Material In The Device Enables The Lowering Of Bandgap At The Source/Channel Interface Which Increases The Tunnelling Rate Of Charge Carriers And Hence Improves The Drain Current (Ids) And Transconductance (Gm), Resulting In Better Current Driving Capability Of The Device And Use Of Dual Material Of Different Work Functions To Control Gate Reduces Ambipolar Nature. The Proposed Device (DMCG-HCPTFET2) Hence Resolves The Fabrication Issues Of Doping Profile Complexity, Thermal Budget And Is Also Cost Effective.

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