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A 65nm Technology CMOS Inverter

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Abstract *-The inverter is the backbone of any digital circuit which can perform Boolean operation on the single input variable. At present world low power device design and its implementation have got a significant role in the field of nano -electronic circuits. In this paper we have optimized the CMOS inverter design in 65nm technology and verified its operation using cadence virtuoso tool.*
Key Words: *CMOS, p-MOS, n-MOS, threshold voltage Vt , Noise margin ,PDP.*

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I. Introduction

The inverter is the most fundamental logic gate that can perform a Boolean operation on a single input variable. The CMOS inverter consists of an n-mos and a p-mos transistor operating in complementary manner. It behaves like a complementary push pull in the sense for the high input (on state), the p- mos transistor is off and the n-mos transistor act as a load and for the low input (off state) the p-mos transistor drives (pulls up) the output load while the n- mos transistor is off. The CMOS inverter has two major advantages, First the steady state power dissipation of CMOS inverter circuit is negligible (except for a small leakage current) so it offers low power dissipation and second the voltage transfer characteristic (VTC) exhibit a full output voltage swing between 0V and VDD i.e. will operate over a wide range of source and input voltages (provided the source voltage is fixed).Besides this it shows a high noise margin and has relatively high speed of operation [1].It is also known for the amplification of analog signal when it is operated at the middle of the VTC ,when both the transistor is in the saturation mode.

1.1 CMOS inverter structure

The CMOS inverter is realized by the series connection of a p-MOS and n-MOS. Both their gates are connected to the input line and their drains are connected to the output. For avoiding the short channel effect the body of both the MOS is connected to their respective sources.

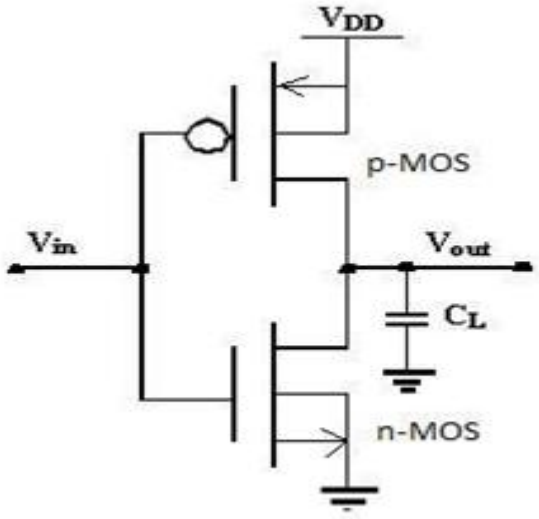

Fig 1: Structure of CMOS inverter

1.2 CMOS inverter operation

The operation of the circuit can be explained with the help of diagram followed by the table:

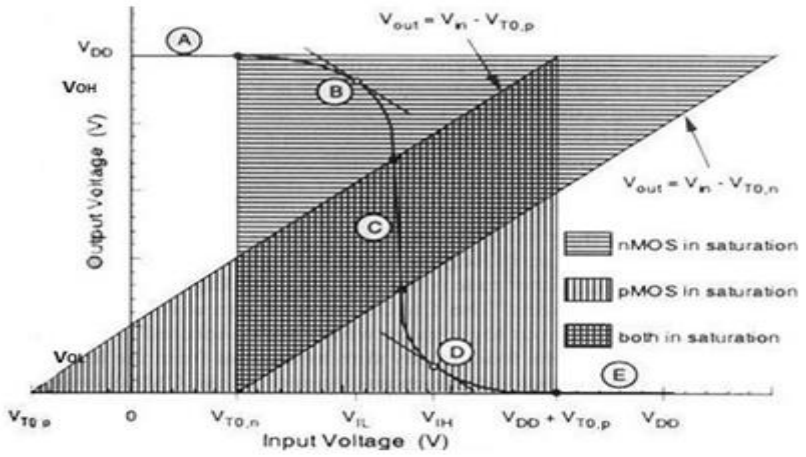

Fig 2: Operating region of n-MOS and p-MOS transistor [1]

Table -1: Operation of the CMOS inverter

Region	Vin	Vout	n-mos	p-mos	Comm.-ents
A	< VTo,n	VOH	Cut-off	Linear	Output~VDD
B	VIL	High ~VOH	Saturation	Linear	Slope=-1
C	Vth	Vth	Saturation	Saturation	VIN = VOUT
D	VIH	Low ~VOL	Linear	Saturation	Slope = -1
E	>(Vdd +VTo,p)	VOL	Linear	Cut-off	Output~ 0V

1.3 Noise Margin

It is the amount of noise that a CMOS circuit could withstand without compromising the operation of circuit.
Low Noise margin NML=VIL-VOL
High noise margin NMH= VOH-VIL
For an ideal CMOS Inverter Noise margin NM=NML=NMH=VDD/2

1.4 Power dissipation

The static power dissipation of the CMOS inverter is very negligible as it does not draw any significant current from the power source in both the steady state operating points
.There is a small current which is actually a reverse leakage current due to short channel effect.
It is given by Isat * VDD
The dynamic power dissipation occurs during switching from high to low and vice versa and during this period CMOS inverter conducts a significant amount of current.
Dynamic power (PD) = CL* VDD^2* frequency
So power is a function of load capacitance (CL), power supply and frequency of operation. A reduction of any one factor will reduce the power consumption and thus reduce the heat developed in the device.
The total power dissipation is the sum of both the powers which is very less with major contribution of dynamic power. This makes CMOS technology attractive in low power and high-density applications.

2. Simulated Result

The conventional CMOS is designed using TSMC 65nm PDK in cadence virtuoso tool with WP/WN ratio of ~2.3, operating at 1V VDD supply.

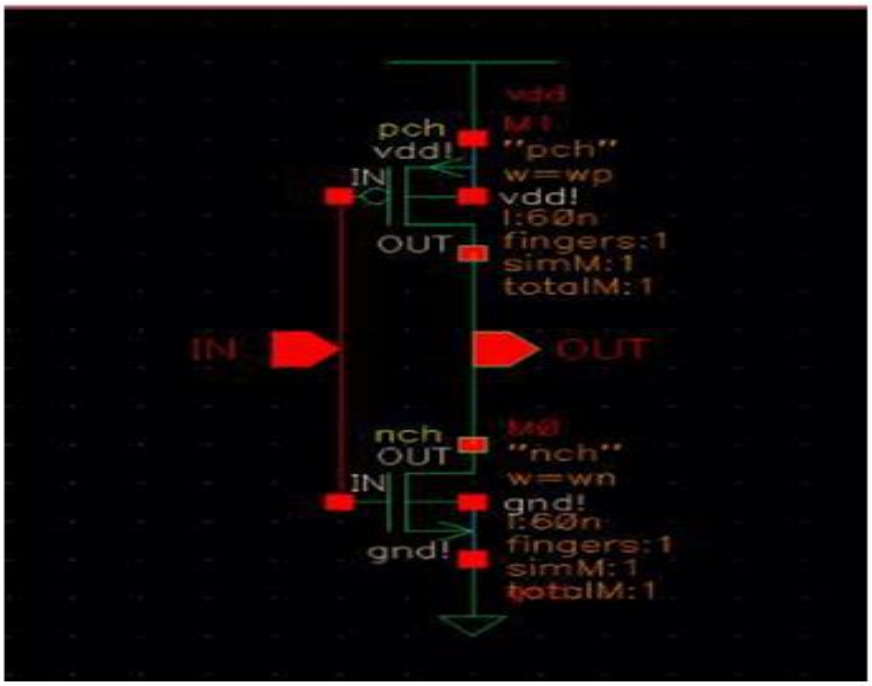

Fig:3 Schematic diagram of CMOS inverter

We assume that all parasitic capacitances are lumped together into one single capacitor CL [2]. The CMOS inverter is operated with a square pulse input waveform.

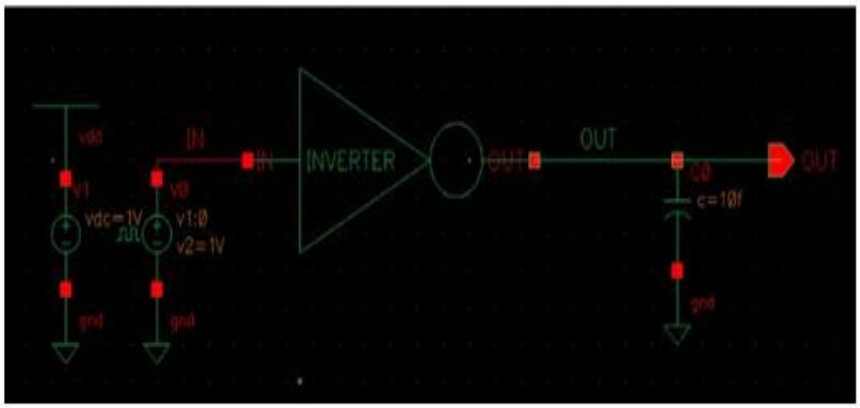

Fig 4: Transient analysis of CMOS inverter with CL as as load

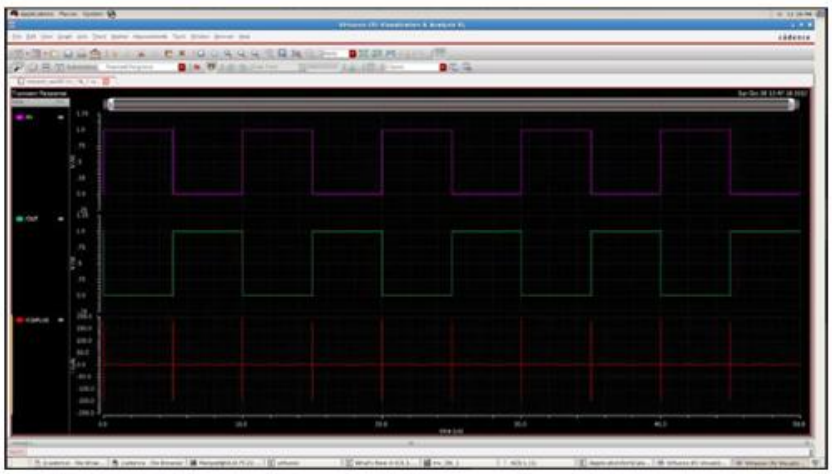

Fig 5: Transient behavior of CMOS inverter (i) VIN (ii)VOUT (iii) IC

The capacitance current Ic is almost negligible in the static region and is significant during transitions. This dynamic current occurs as a result of the p-MOS and n-MOS simultaneously transitioning through their linear region. These two continuous current peaks during transition in opposite direction aren't equal; since the total current being drawn through the p -MOS is being split between the output path and the n-MOS path.

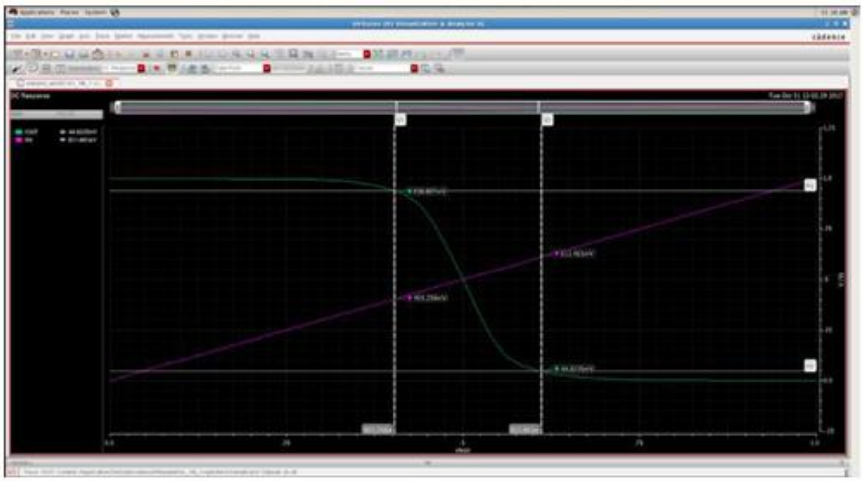

Fig 6 : VTC of the CMOS inverter.

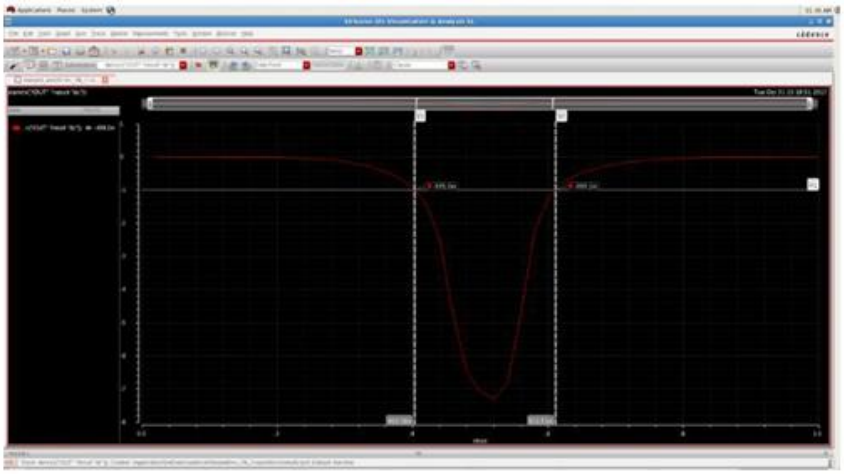

Fig 7: VTC derivative curve of CMOS inverter.

The highlighted derivative value represents the points where the slope of VTC is exactly -1 i.e. points of VIL and VIH.

II. Conclusions

In this paper an optimized COMS inverter is designed with 65 nm technology .The dc and the transient analysis of the purposed designed is verified using Cadence virtuoso tool. The power dissipation shown by the CMOS inverter is only a few nW (~1.5) so it gives a less heat stress and thus a good reliability. Less power consumption also extend the battery life in battery powered system. The CMOS inverter is used in analog circuits, digital circuits, ring oscillator etc. Some interesting issue like PDP, rise and fall time etc remains to be investigated.

Acknowledgement

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